
**Voltage Control System Demonstration Project
Phase 1 – Testing of a D-SVC**

Report for D-SVC operation in AVR mode
(9th July– 1st August 2012)



Western Power Distribution

Prepared by:

HITACHI
Inspire the Next



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Revision 01

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Executive Summary

This draft report confirms that the D-SVC suppresses voltage fluctuation on a rural 11kV overhead network with wind turbines connected close to the split point. The period covered by this report is between 9th July and 1st August (20 days). During that time period the SVC was operated in AVR (Automotive Voltage Regulation) mode. Future activity in this project will explore the impact on voltage of operating the SVC in other modes with respect to different combinations of wind output and line load.

The key points of this report include:

- Voltage fluctuation suppression at the D-SVC installation point
- Voltage fluctuation suppression at other points on the feeder

We confirm that the measured and approximated (i.e. calculated) voltage fluctuation suppression are almost the same. The measured voltage fluctuation suppression is obtained by measuring voltage when the D-SVC is operating and when switched off. When the phase to neutral base voltage is 6350[V] and D-SVC reactive power output was 380[kVAr], the measured deviation of voltage was 43.5[V]. On the other hand, the calculated deviation of voltage was 45.1[V] from the line impedance and D-SVC reactive power. (Appendix A Formula (A.1))

Using the data generated from this project it is now possible to estimate the appropriate rating of a D-SVC with respect to the amount of voltage fluctuation to be suppressed (based on system impedance).

1.0 Background

As Distributed Generators (DG) become more common, the growing number of connections to distribution lines will cause voltage problems (specifically high or low voltage) due to the variable power output of the DG as a majority of DG are weather-dependent. In turn this can affect the efficiency and capacity of the distribution network.

Traditional solutions to combat these issues include auto-transformers and reinforcement of the network. The latter can be costly and time-consuming, although in some cases this may be the only possible solution where capacity is concerned, and the former, given its electro-mechanical nature is slow to react to changes on the network. Furthermore, some DNOs wonder about the total cost of maintenance in locations where the auto-transformer is continuously tapping.

New innovation solutions such as the D-SVC are able to react quickly to changes on the network, are more economical and have a smaller footprint. When optimised, these types of devices should reduce voltage fluctuations and increase the capacity of existing lines to allow additional DG connections without the need for network reinforcement.

2.0 Objectives and Scope

This project aims to address the issue of fluctuations seen in long distribution lines in a rural area with DG (in the form of Wind Turbines) connected. The objective is to determine the effectiveness of D-SVCs (Static VAr Compensator for Distribution Networks) as a system to control voltage on 11kV rural networks.

Phase 1 comprises the testing of a single D-SVC, providing feed-back for the development of a D-VQC (Voltage and Reactive Power (Q) Control System) that will be utilised. Phase 2 will explore the networking and optimisation of multiple D-SVCs across two primary substations.

This report analyses data obtained from monitoring units installed across several locations on the feeder whilst the D-SVC is operating in AVR (Automatic Voltage Regulation) mode as part of phase 1 of the project. Revision 2 of this report will include analysis of data collected during other D-SVC modes of operation being tested. The data analysis will inform the effectiveness of the D-SVC at each of the monitoring points, and a comparison of simulated and actual results will be made.

3.0 Test Schedule

After a re-commissioning exercise with WPD was performed on 23rd and 24th May (refer to HITACHI-WPD - D-SVC summary report 20120625.pdf), the D-SVC was officially restarted for continuous testing from 9th July after adjusting network protection settings.

The test schedule plan is to operate and test the D-SVC in several different operation modes:

- AVR – Automatic Voltage Regulation mode
- ARV – Average Reference Voltage mode
- SFV – Short Term Fluctuation of Voltage mode

Each mode will be operated continuously for approximately 2 weeks before changing to the next mode. During mode change the D-SVC will remain off for an hour in order to collect network data whilst the D-SVC is off – this data will be used as confirmation of D-SVC effectiveness.

Although this report will only analyse the data collected during AVR mode, the table below details the operational status of the D-SVC from May to date.

Table 3.1: Test Schedule

Date	D-SVC operation
24 th May	D-SVC off after WPD and Hitachi joint test
9 th July	D-SVC on in AVR mode after resetting of WPF protection system
1 st August	D-SVC off, switched to ARV mode and restarted
22 nd August	D-SVC off, switched to AVR mode and restarted

4.0 Test Feeder

Figure 4.1 shows the Test Feeder. Sub.net, which is WPD’s monitor system, is located at five nodes shown in Table 4.1.

D-SVC setting is as follows;

- The operation mode is AVR mode.
- The Value of Vref, which is the voltage reference, is 0.98 [PU].
-

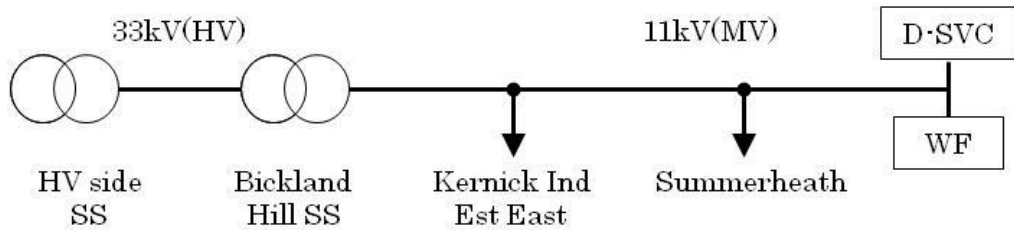


Figure 4.1: Test Feeder

Table 4.1: Test Feeder

No	Node	Line Impedance from HV side SS (400[kVA] base)	Sub.net Location	Transformer	
				Capacity	Transformation ratio
1	Bickland Hill SS	0.291[%]	LV	No data	11000/433
2	Kernick Ind Est East	0.478[%]	LV	500[kVA]	11000/433
3	Summerheath	0.529[%]	LV	200[kVA]	11000/433
4	Roskrow WF	0.748[%]	MV	None	None
5	D-SVC	0.748[%]	LV	500[kVA]	11000/415

5.0 Results

5.1 Low resolution data

Using sub.net monitoring units, we recorded the 10 minute-average data (low resolution) from 24th May to 1st August. The graphs included in this section are generated from data collected from Monday 30th July when D-SVC was in AVR mode – this data is representative for any weekday during the above time period; please refer to Appendix C for summarized weekly data.

The value of voltages in these graphs is phase voltage. The plus Q means lead Q (or capacitive Q), and the minus Q means lagged Q (or inductive Q) from the point of view of power system. Time in these graphs is written in UTC (summer time is not accounted for in the GPS clock of sub.net monitoring units).

(1) D-SVC

As seen from Figure 5.1.2, the largest Q fluctuation in an hour was observed from 6:30 to 7:30. The deviation of Q is approximately 700[kVar], from lead 400[kVar] to lagged 300[kVar]. The base voltage in Figure 5.1.1 is 230[V].

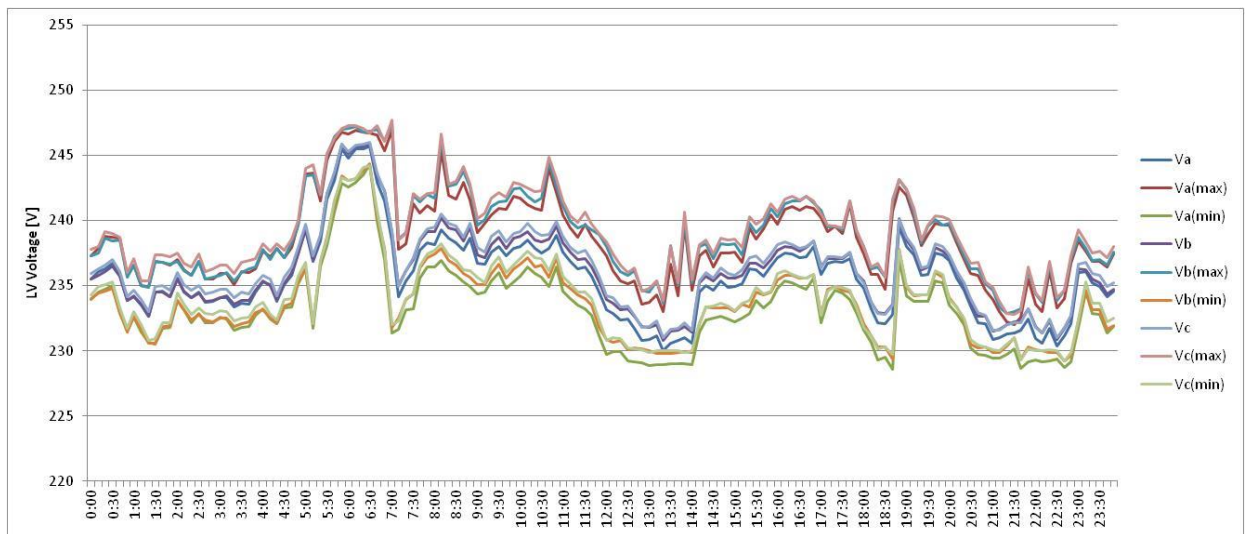


Figure 5.1.1: V recorded from D-SVC sub.net 0:00-23:50 30th July

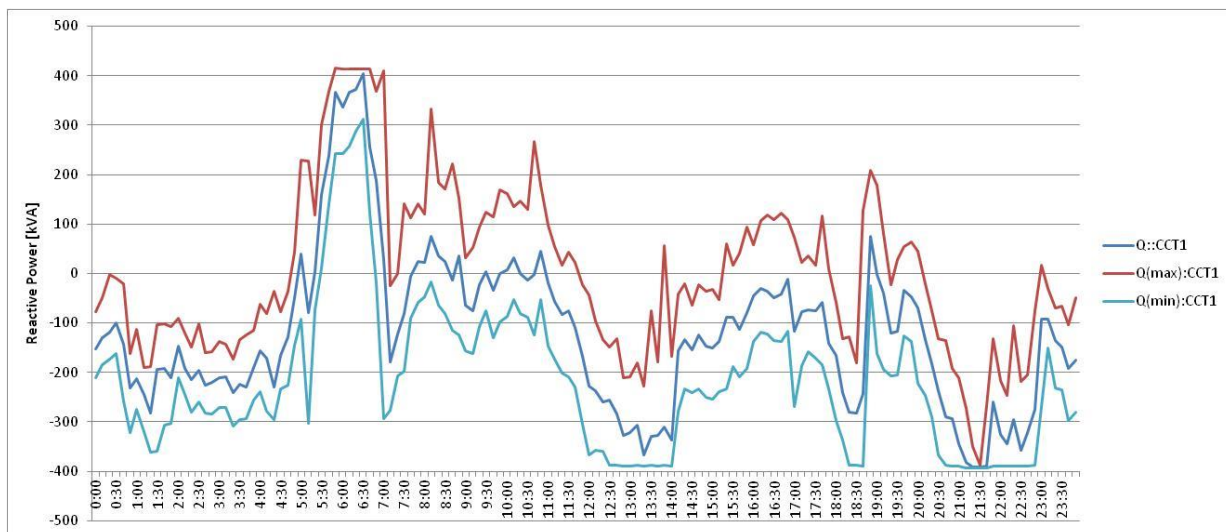


Figure 5.1.2: Q recorded from D-SVC sub.net 0:00-23:50 30th July

(2) Roskrow WF

The base voltage in Figure 5.1.3 is 6350[V].

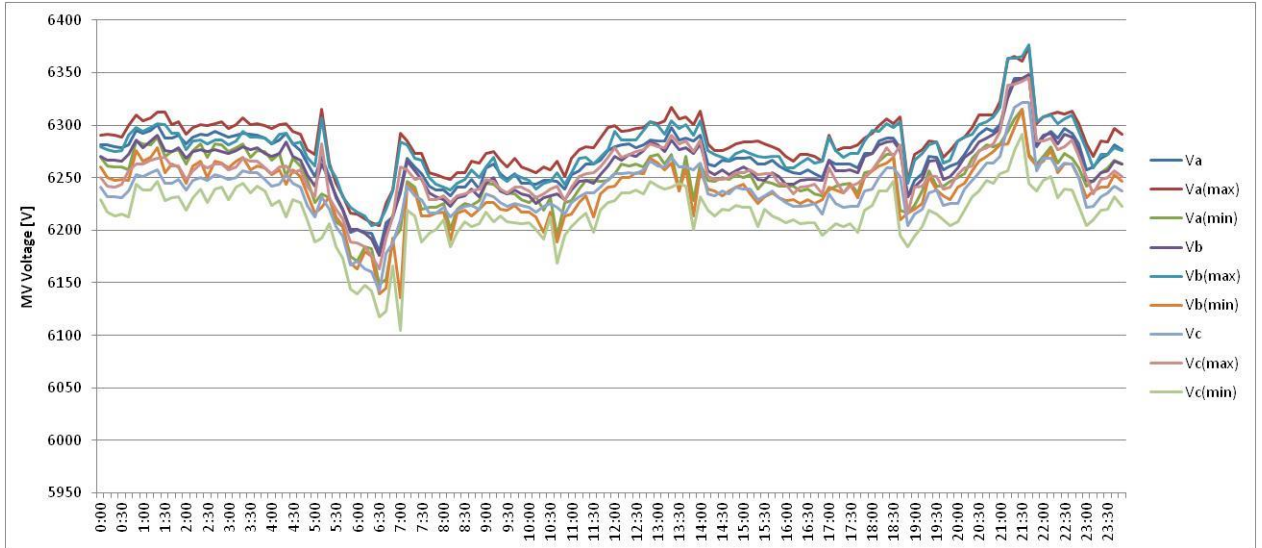


Figure 5.1.3: V recorded from Roskrow WF sub.net 0:00-23:50 30th July

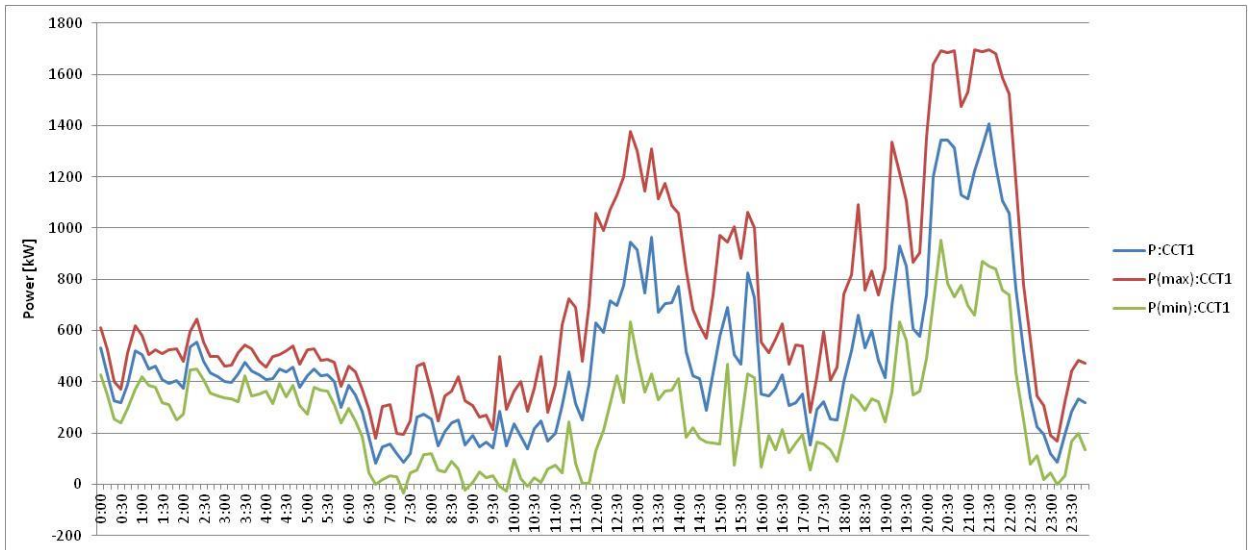


Figure 5.1.4: P recorded from Roskrow WF sub.net 0:00-23:50 30th July

(3) Bickland Hill SS

As seen in Figure 5.1.5 the LV voltage is almost constant from 0:00 to 4:30 in midnight. On the other hand, from 6:30 to 7:30 in the morning, the largest voltage deviation in an hour was observed. The base voltage in Figure 5.1.5 is 230[V].



Figure 5.1.5: V recorded from Bickland Hill SS sub.net 0:00-23:50 30th July

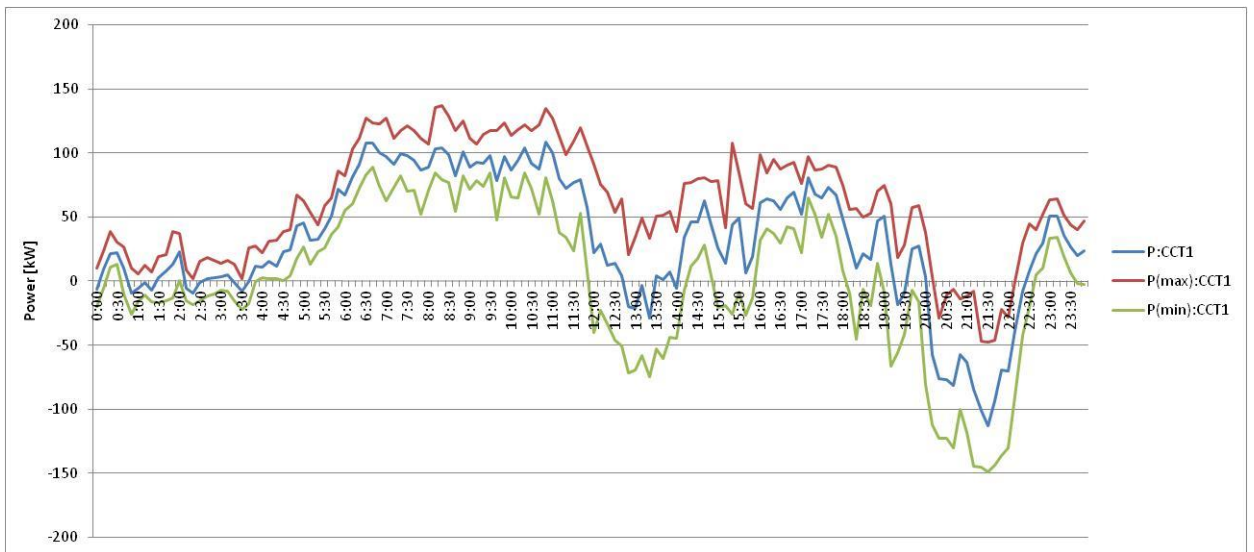


Figure 5.1.6: P recorded from Bickland Hill SS sub.net 0:00-23:50 30th July

(4) Kernick Ind Est East

As seen in Figure 5.1.8, the power consumption is concentrated from 6:00 to 17:00 on weekdays. Thus, the LV voltage was lowered during this term in Figure 5.1.7. In weekend, there is almost no power consumption. The base voltage in Figure 5.1.7 is 230[V].

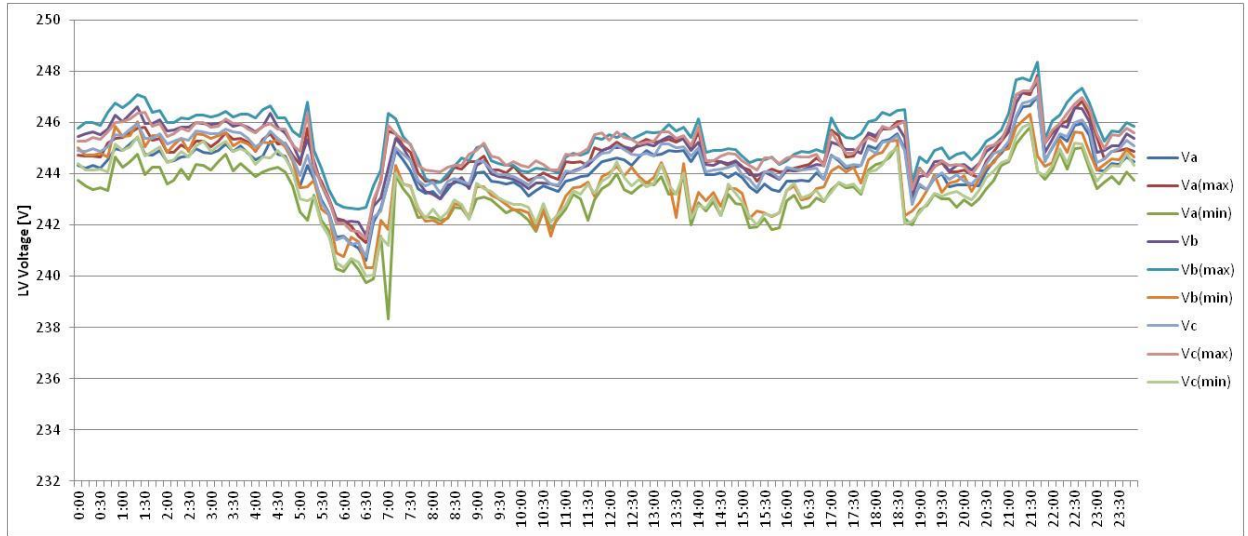


Figure 5.1.7: V recorded from Kernick sub.net 0:00-23:50 30th July

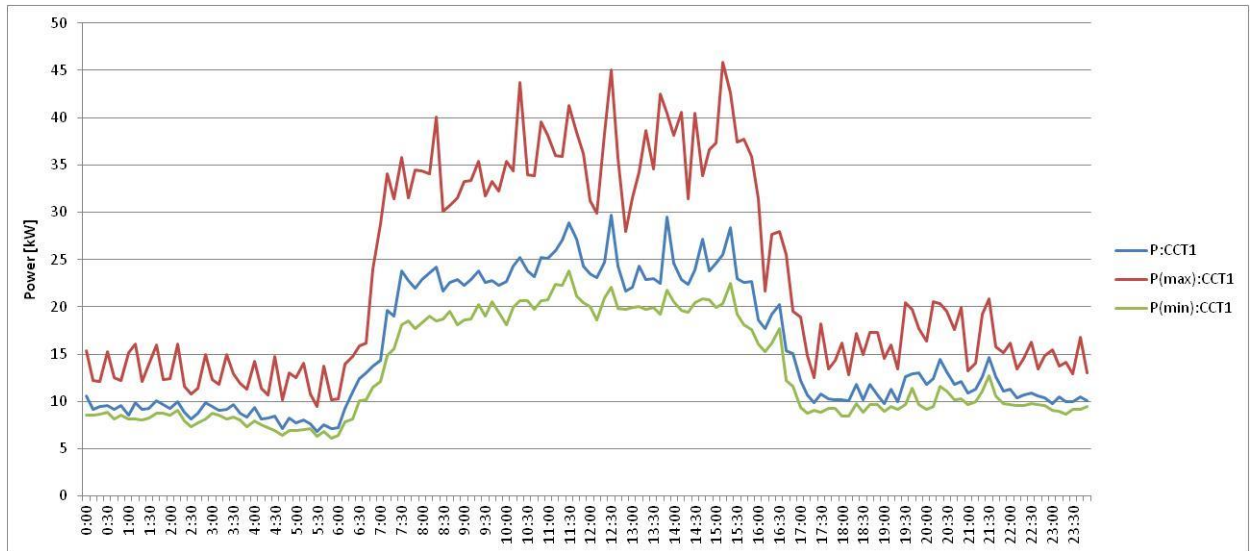


Figure 5.1.8: P recorded from Kernick sub.net 0:00-23:50 30th July

(5) Summerheath

As seen in Figure 5.1.10, two low peaks of power consumption are observed at 8:00 and 18:00 on weekdays. There is almost no power consumption from 0:00 to 5:00 in midnight. The value of Va and Vb in Figure 5.1.9 are almost 0. Possible reasons are related to Sub.net fuse and problems with the sensors. The base voltage in Figure 5.1.9 is 230[V].

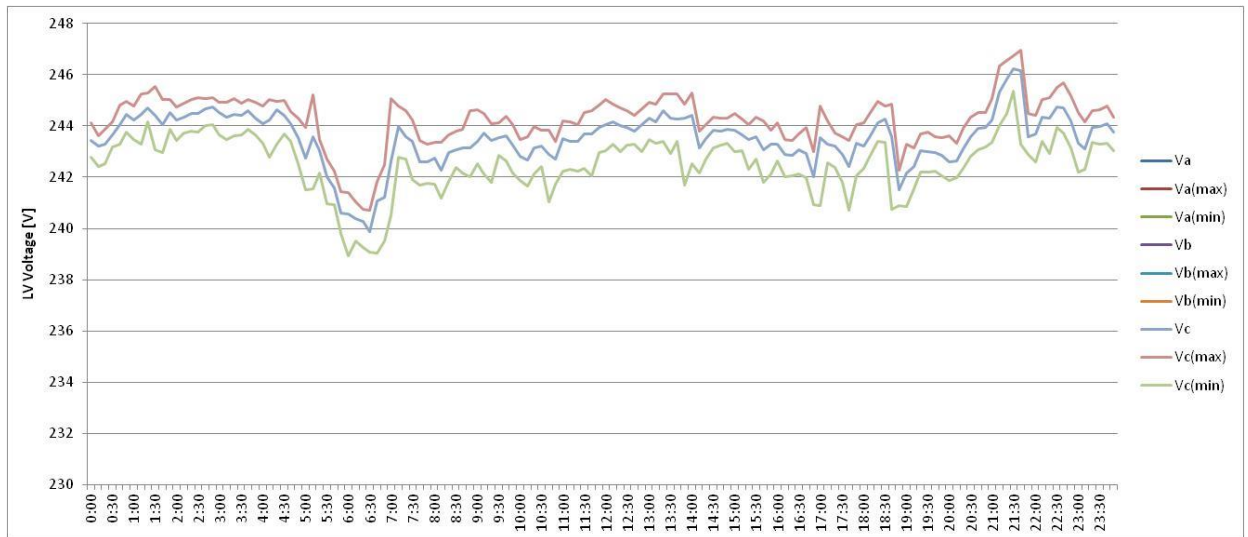


Figure 5.1.9: V recorded from Summerheath sub.net 0:00-23:50 30th July

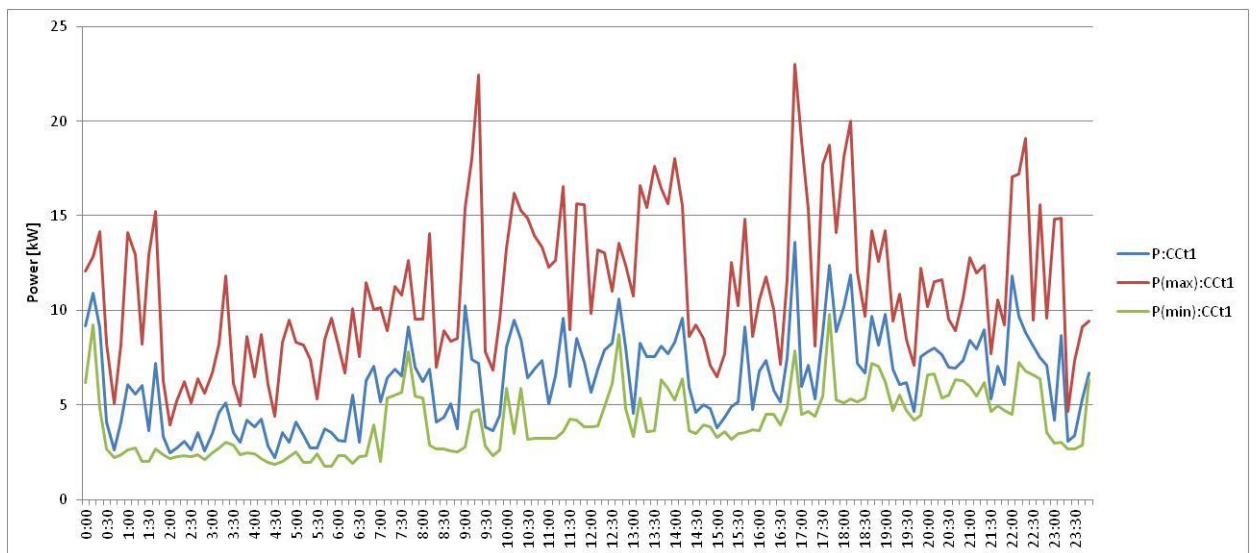


Figure 5.1.10: P recorded from Summerheath sub.net 0:00-23:50pm 30th July

5.2 High resolution data

The purpose of this project is to investigate the voltage fluctuation suppression by D-SVC. Thus, it is desirable to obtain the data when the deviation of Q of D-SVC output is large. As shown in Figure 5.1.5, Q of D-SVC fluctuated from lead 400kVar to lagged 300kVar at 6:30, which is the largest deviation on 30th July. Data covering this time period was downloaded and analysed. Included in this section are these graphs, which show only 3000[sec] because of restrictions imposed by Microsoft Excel

The value of voltages in these graphs is phase voltage. The plus Q means lead Q (or capacitive Q), and the minus Q means lagged Q (or inductive Q) from the point of view of power system.

(1) D-SVC

The base Voltage in Figure 5.2.1 is 240[V].

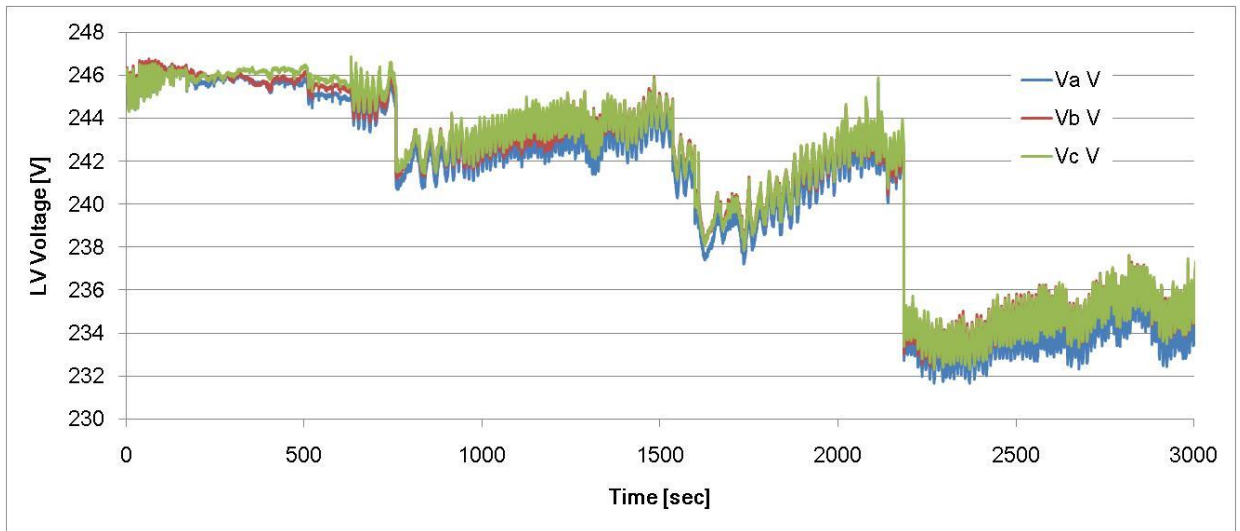


Figure 5.2.1: V recorded from D-SVC sub.net 6:30-7:20 30th July

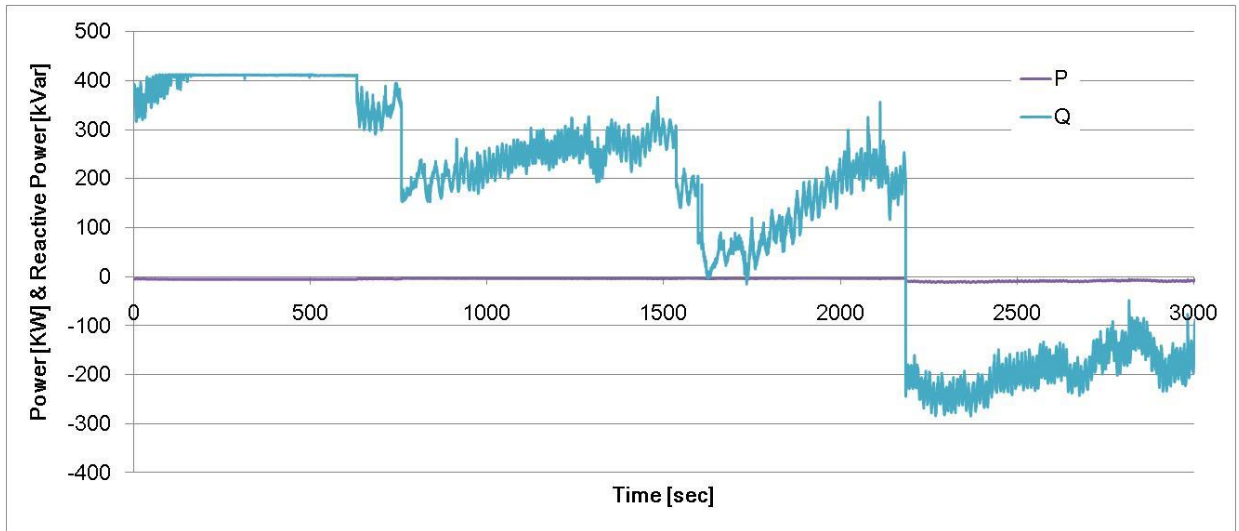


Figure 5.2.2: P and Q recorded from D-SVC sub.net 6:30-7:20 30th July

(2) Roskrow WF

The base voltage in Figure 5.2.3 is 6,350[V].

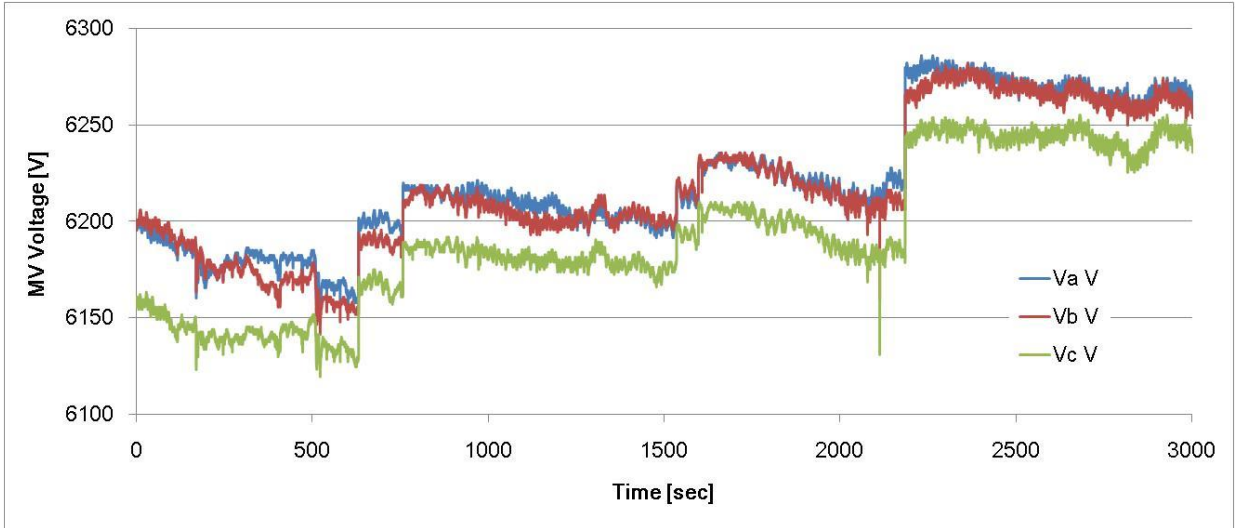


Figure 5.2.3: V recorded from Roskrow WF sub.net 6:30-7:20 30th July

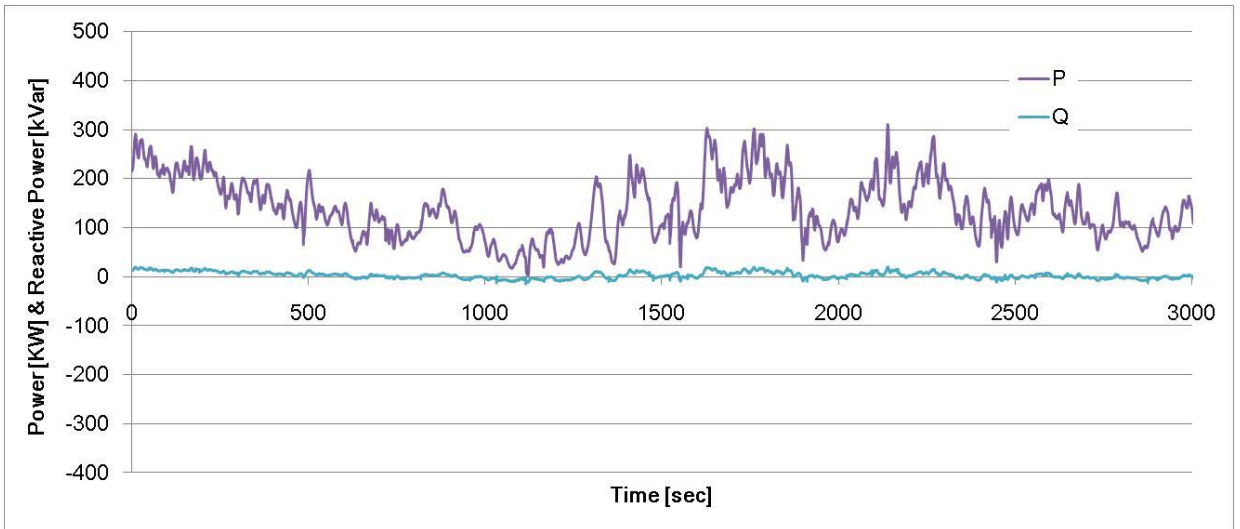


Figure 5.2.4: P & Q recorded from Roskrow WF sub.net 6:30-7:20 30th July

(3) Bickland Hill SS

The base voltage in Figure 5.2.5 is 6,350[V].

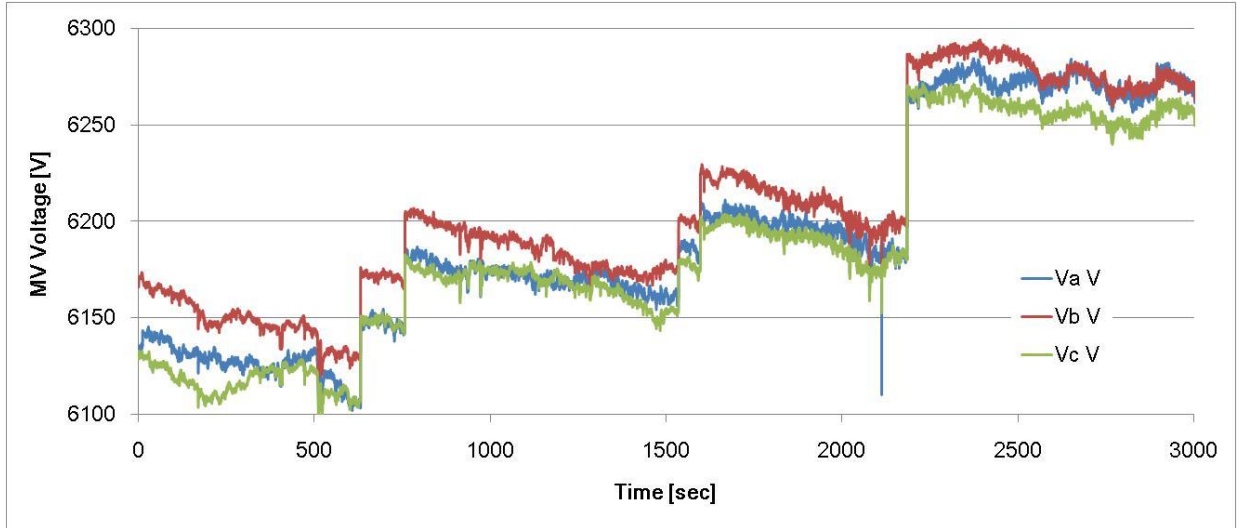


Figure 5.2.5: V recorded from Bickland Hill SS sub.net 6:30-7:20 30th July

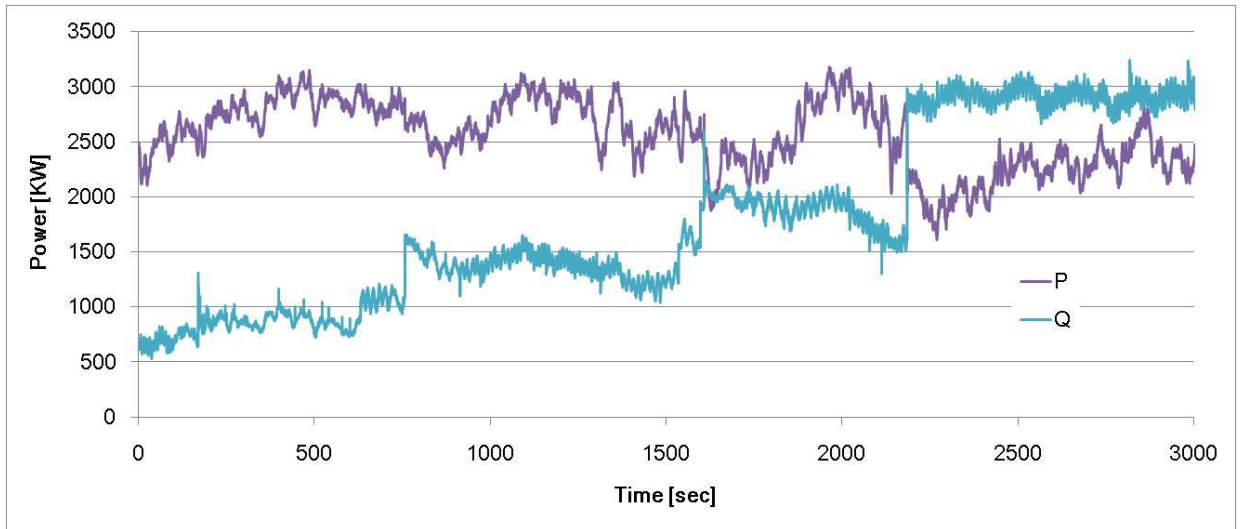


Figure 5.2.6: P & Q recorded from Bickland Hill SS sub.net 6:30-7:20 30th July

6.0 Analysis

6.1 D-SVC Q output

In order to check D-SVC integrity, we confirmed D-SVC decreases lagged Q output with increase in HV voltage at WF in AVR mode. Figure 6.1.1 shows Q at D-SVC in Figure 5.2.2 and MV voltage (V_c) at WF in Figure 5.2.3.

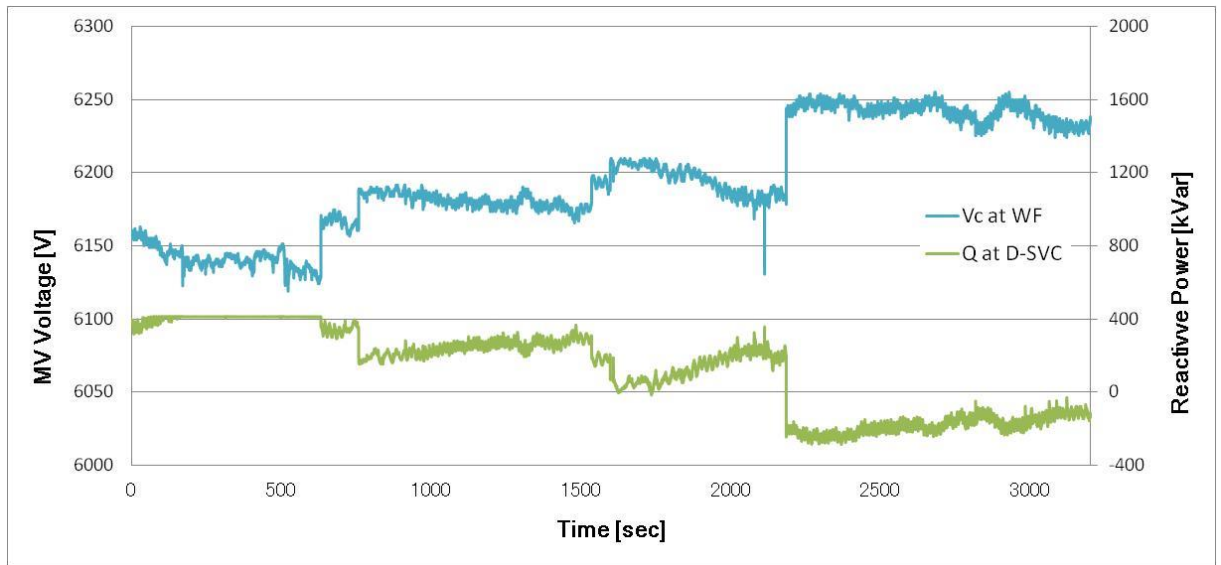


Figure 6.1.1: V at WF and Q at D-SVC 6:30-7:20 30th July

Figure 6.1.2 shows correlation between Q at D-SVC and HV voltage at WF in Figure 6.1.1. The correlation coefficient is -0.982, which means clear negative correlation. When Q is equal to 1 in Figure 6.1.2, there are a several outliers from negative correlation because of Q saturation. It will be resolved if D-SVC has more capacity.

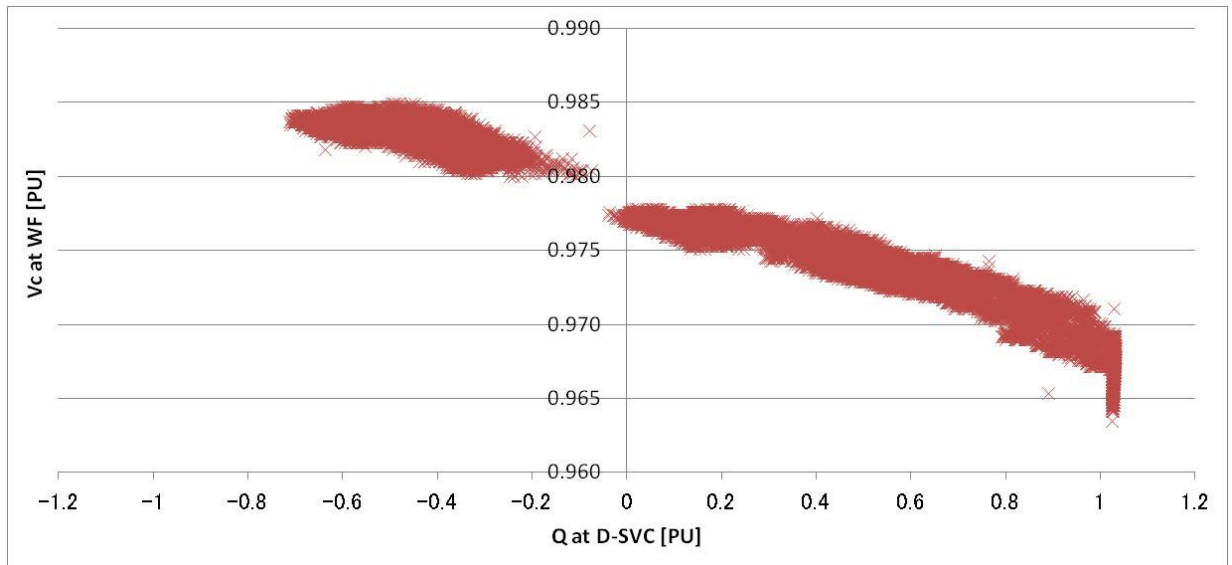


Figure 6.1.2: Correlation between V_c at WF and Q at D-SVC

Substituting V_c at WF, V_c at D-VQC and Q at WF and line impedance in formula (A.1) in Appendix A, V_c during D-SVC off can be calculated. Figure 6.1.3 shows this calculation results. At 2200[sec], when MV voltage changes from 6180[V] to 6250[V], D-SVC changes output from lead Q to lagged Q. Given $V_{ref} = 0.98[PU] = 6223[V]$ (phase voltage), this D-SVC output change can be said to be appropriate.

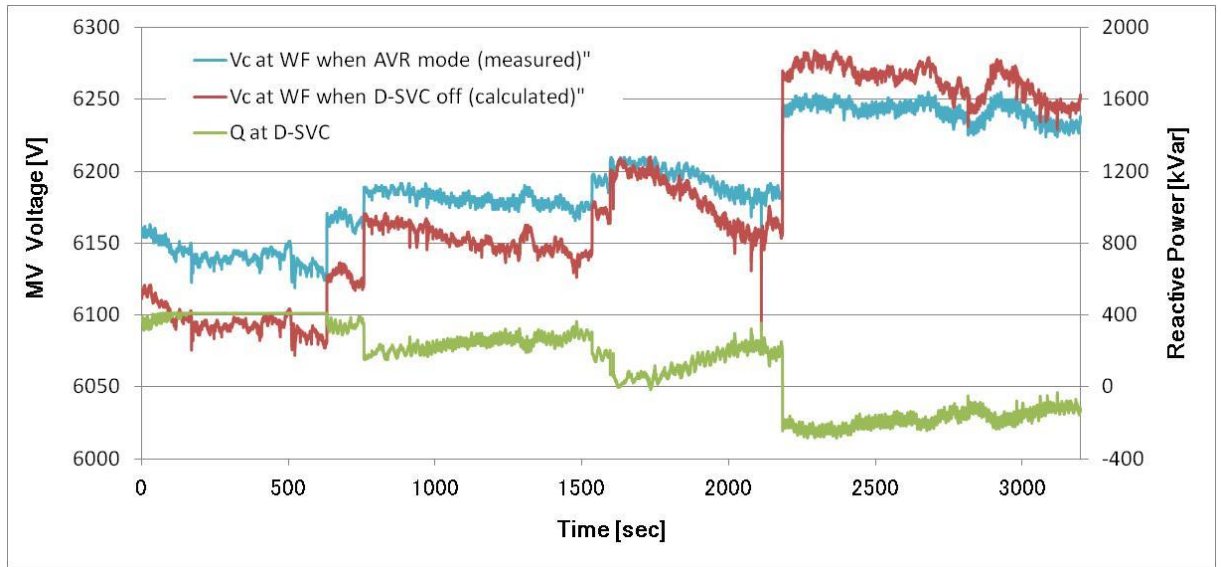


Figure 6.1.3: Calculated V_c at WF when D-SVC off

We performed the same evaluation using data from 19th July, giving similar results. Please refer to Appendix B for this evaluation.

6.2 Effect at consumer node

(1) Voltage fluctuation range

We confirm the voltage fluctuation suppression at Summerheath, Kernick Ind Est East and Roskrow WF by calculating the voltage fluctuation range.

The voltage fluctuation range, V_{range} as shown in Figure 6.2.1, can be obtained by subtracting minimum voltage from maximum voltage. The average of V_{range} is calculated from data of weekdays from week of 2nd July and 16th July for the case of D-SVC off and the case of AVR mode (SVC on), respectively.



Figure 6.2.1: Definition of V_{range}

Figure 6.2.2 shows the average of V_{range} when D-SVC off and AVR mode. During “D-SVC off”, the closer a node is to the SS, the smaller the V_{range} experienced at the node. During AVR mode, the average of V_{range} resembles the inverse of a “smile curve”. That means, the closer a node is to D-SVC, the greater is the suppression of voltage fluctuation. This is because the voltage drop or swell caused by Q is linear to inductance to the node.

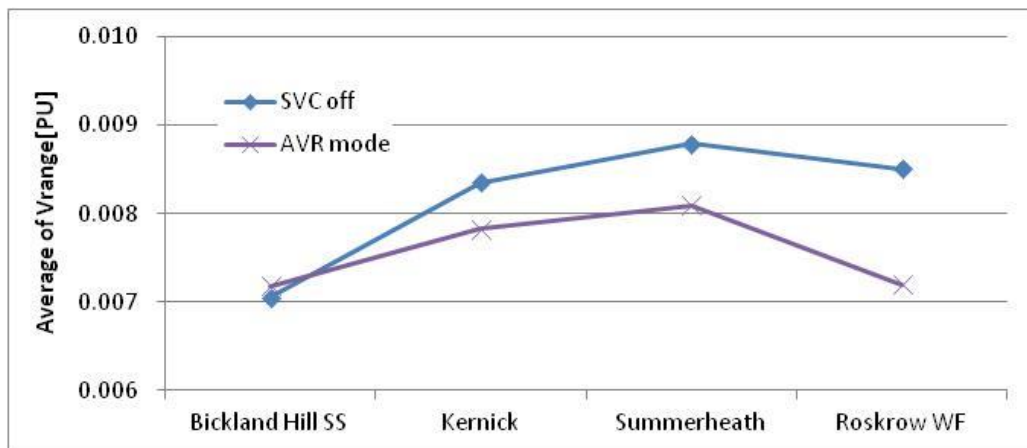


Figure 6.2.2: Average of V_{range}

(2) Voltage deviation

Using the formula (A.1) in Appendix A, LV voltage at consumer node during D-SVC off can also be calculated. For example, Figure 6.2.3 shows the calculated V_c at Kernick. As seen in 500[sec], V_c is put up by 1.0[V] by D-SVC, which is the maximum voltage deviation at this node.

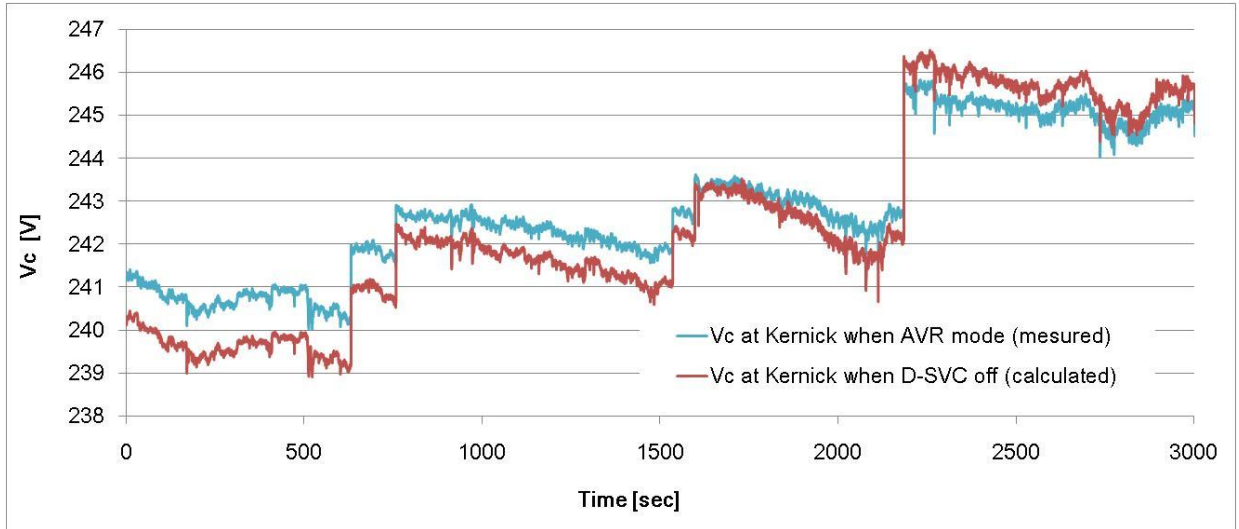


Figure 6.2.3: V_c at Kernick 6:30-7:20 30th July

6.3 Effect at Roskrow WF

The voltage duration caused by D-SVC, depends on the impedance of feeder and D-SVC capacity. In this project, the impedance from SS to WF is 0.748[%] (@400[kVA]). The capacity of D-SVC is 400[kVar].

We can obtain almost the largest voltage deviation when we switched from AVR mode to “D-SVC off” at 1:05 on 1st August. Figure 6.3.1 shows that MV voltage duration caused by D-SVC is approximately 43.5 [V] given the capacity of D-SVC and the impedance of this feeder.

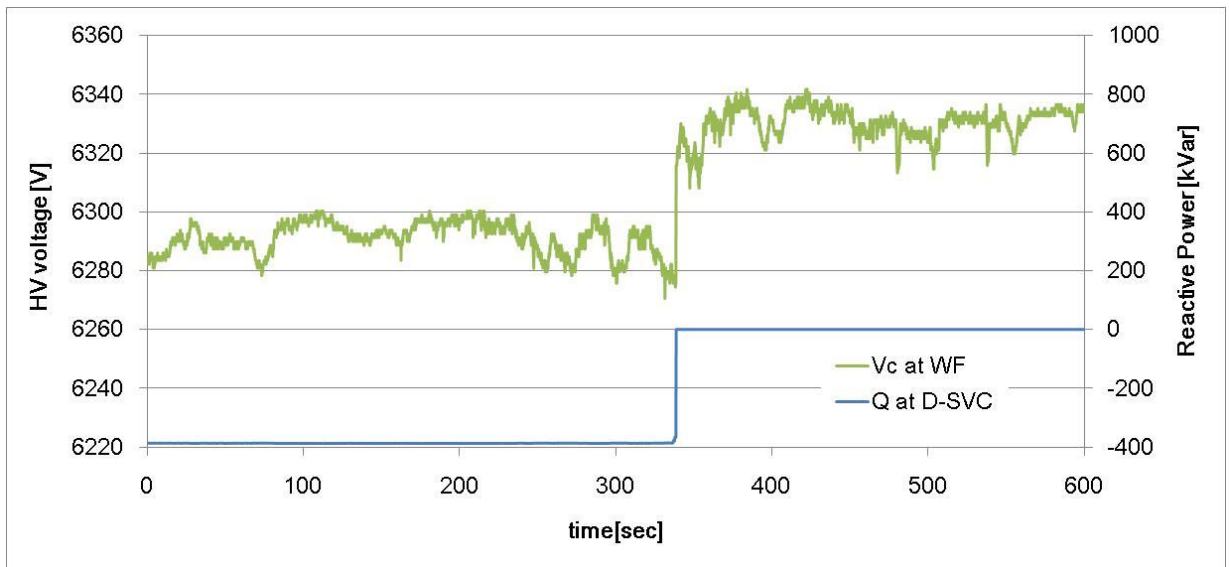


Figure 6.3.1: Vc at WF and Q at D-SVC from 13:00 to 13:10 on 1st August

In the previous report (*1), MV voltage deviation caused by D-SVC is 120[V], which is peak to peak line voltage as shown in Table 6.3.1. Converted to peak to 0 phase voltage, this is 34.9 [V], smaller than the measured result. This requires further investigation. One possible reason is that the simulation result did not include the voltage drop caused by back impedance of Bickland Hill SS.

Table 6.3.1: Comparison Simulation and calculation result with measured result

		Simulation result		Calculation Result from formula (A.1)	Measured Result from Figure 6.3.1
Evaluation method	Vc measurement	Line to Line	Phase to Neutral	Phase to Neutral	Phase to Neutral
	Q at D-SVC [kVar]	-400 to +400	-400 to 0	-380 to 0	-380 to 0
Deviation of Vc at WF [V]		121.0 (*1)	34.9	45.1	43.5

On the other hand, the deviation of Vc calculated by formula (A.1) matches measured result very well as shown in Table 6.3.1. The calculation of the deviation of Vc when Q is changed from -380[kVar] to 0[kVar] is as follows.

$$\text{deviation of } V_c \text{ [pu]} = \left| \left(V + \frac{0.748}{100} \cdot \frac{-380}{1.0} \right) - \left(V + \frac{0.748}{100} \cdot \frac{0}{1.0} \right) \right| = 0.0071$$

where $V_{svc} = 1.0$ [pu]

$$\text{deviation of } V_c \text{ [V]} = 0.0071 \cdot 6350 = 45.1$$

It is difficult to record the Peak to Peak MV voltage deviation on this project. To do so, we have to change D-SVC output from maximum lead Q to maximum lagged Q. We tried this during commissioning but were unable to realise it due to limitations imposed by the protection system.

(*1) Refer to “Voltage Control Systems Demonstration Project : Simulation result of D-STATCOM connected on Feeder 46 out of Falmouth Bickland Hill” pp.19 Table 5.4

Appendix A – How to calculate MV voltage during D-SVC off

If we ignore Q_{svc} to WF, the circuit of the power system with D-SVC can be drawn as Figure A.1. Using MV voltage V at WF, Q at D-SVC and V at D-SVC during AVR mode, we can calculate MV voltage V' at WF during SVC off.

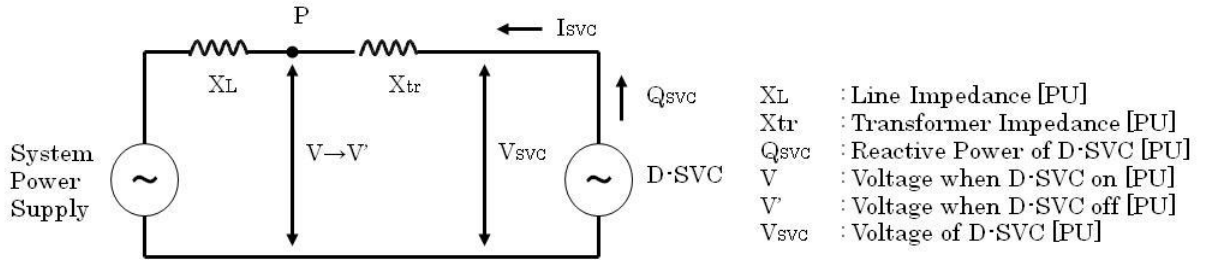


Figure A.1: Circuit of power system

Given that I_{svc} , the current of D-SVC of this circuit, is Q_{svc}/V_{svc} , the voltage drop at point P caused by I_{svc} is as follows

$$\begin{aligned} V_p &= X_L \cdot I_{svc} \\ &= X_L \cdot \frac{Q_{svc}}{V_{svc}} \end{aligned}$$

V , MV voltage at point P during D-SVC off is calculated by subtracting V_p from V , MV voltage at point P during D-SVC on. Thus, V is as follows.

$$\begin{aligned} V &= V' - V_p \\ &= V' - X_L \cdot \frac{Q_{svc}}{V_{svc}} \end{aligned}$$

Therefore, V' is as follows.

$$V' = V + X_L \cdot \frac{Q_{svc}}{V_{svc}} \quad (A.1)$$

For verification of formula (A.1), we calculated MV voltage at WF during SVC off in case of Figure 6.3.3. As seen in Figure A.2. V_c during D-SVC doesn't change like step, even when D-SVC output Q changes from lagged 400[kVar] to 0[kVar] in one single step.

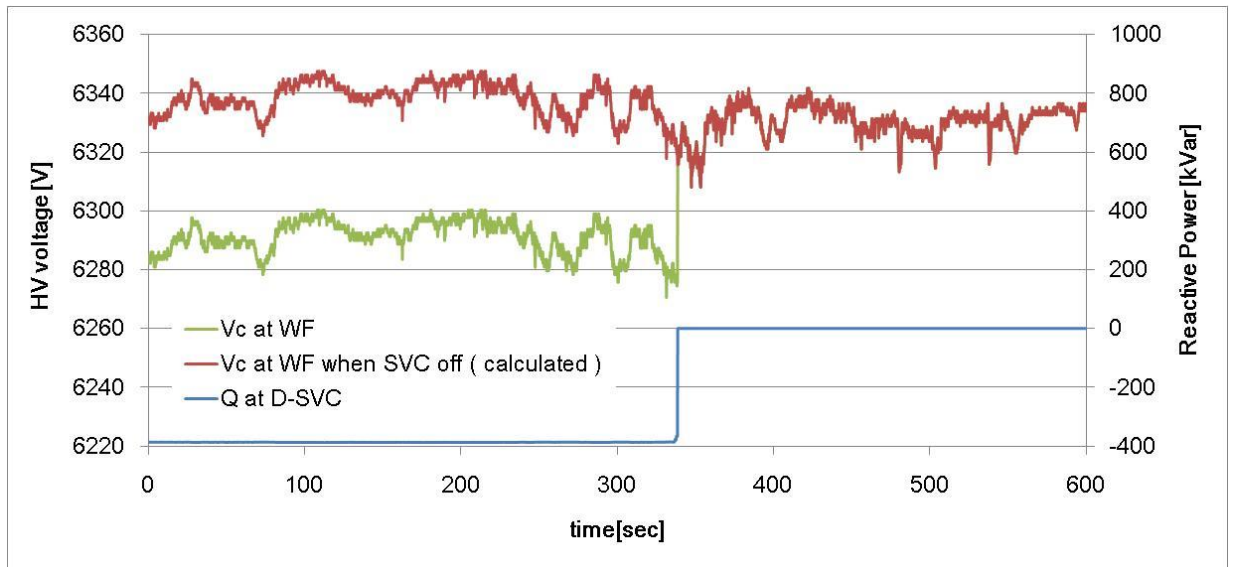


Figure A.2: Calculated Vc at WF during D-SVC off

Appendix B – D-SVC Q output

Using data on 13th July, we performed the same check of D-SVC as section 6.1. Figure B.1 shows Q at D-SVC and MV voltage (Vc) at WF from 1:00 to 2:00 on 19th July.

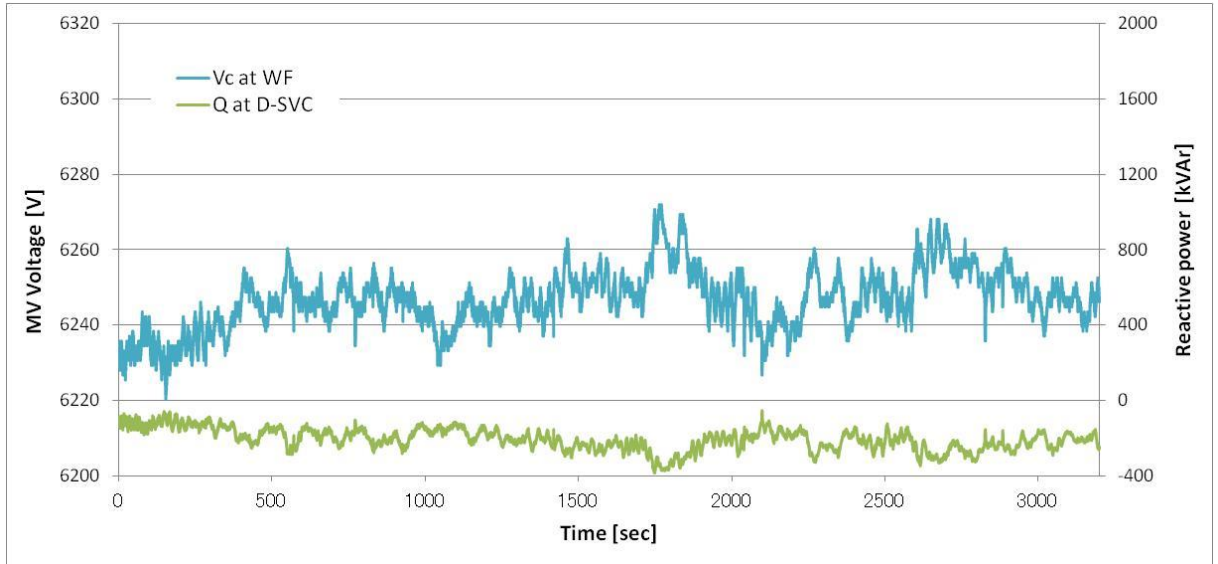


Figure B.1: V at WF and Q at D-SVC 1:00-2:00 19th July

Figure B.2 shows correlation between Q at D-SVC and HV voltage at WF in Figure B.1. The correlation coefficient is -0.849, which means clear negative correlation.

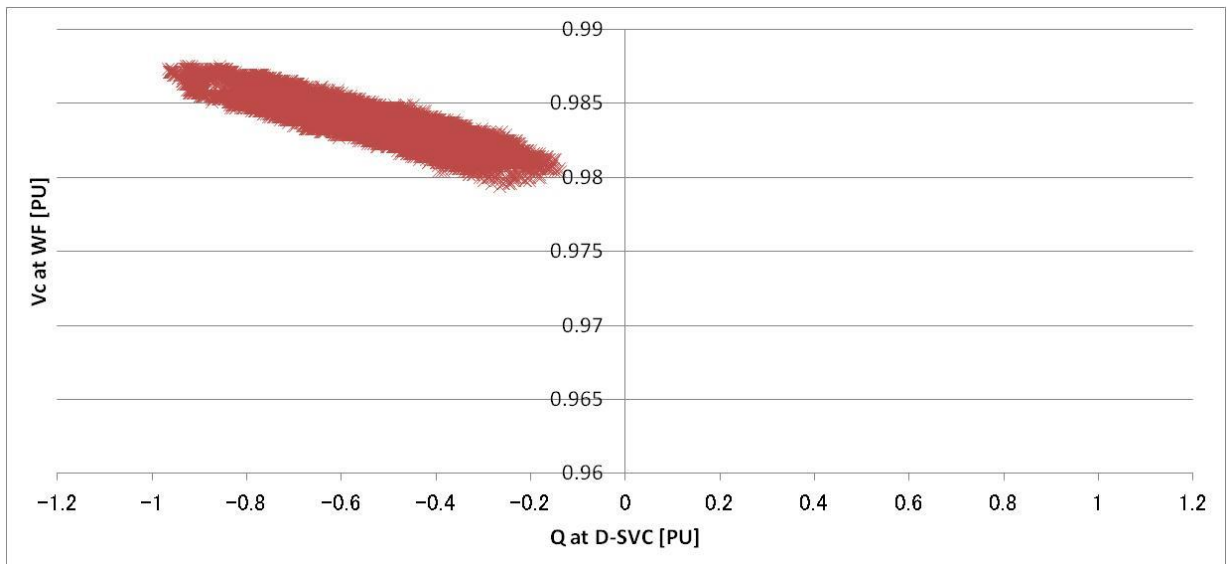


Figure B.2: Correlation between Vc at WF and Q at D-SVC

Substituting Vc at WF, Vc at WF, Q at WF and line impedance in the formula (A.1) in Appendix A, Vc during D-SVC off can be calculated. Figure B.3 shows this

calculation results. By lagged Q, D-SVC lowers the MV voltage. Given $V_{ref} = 0.98[\text{PU}] = 6223[\text{V}]$ (phase voltage), this D-SVC output can be said to be appropriate.

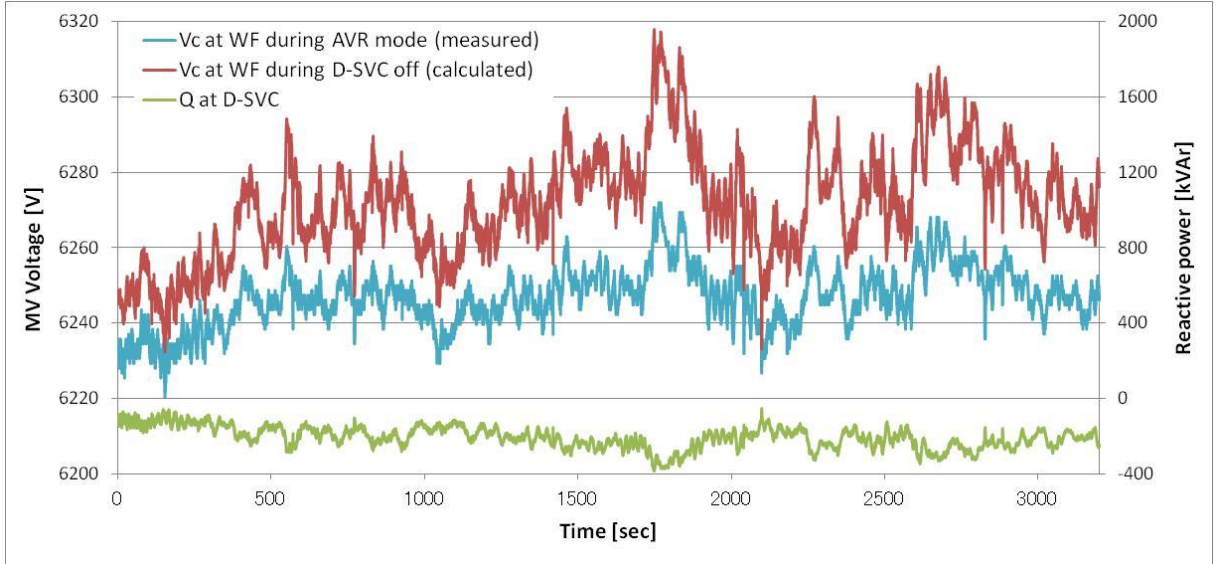
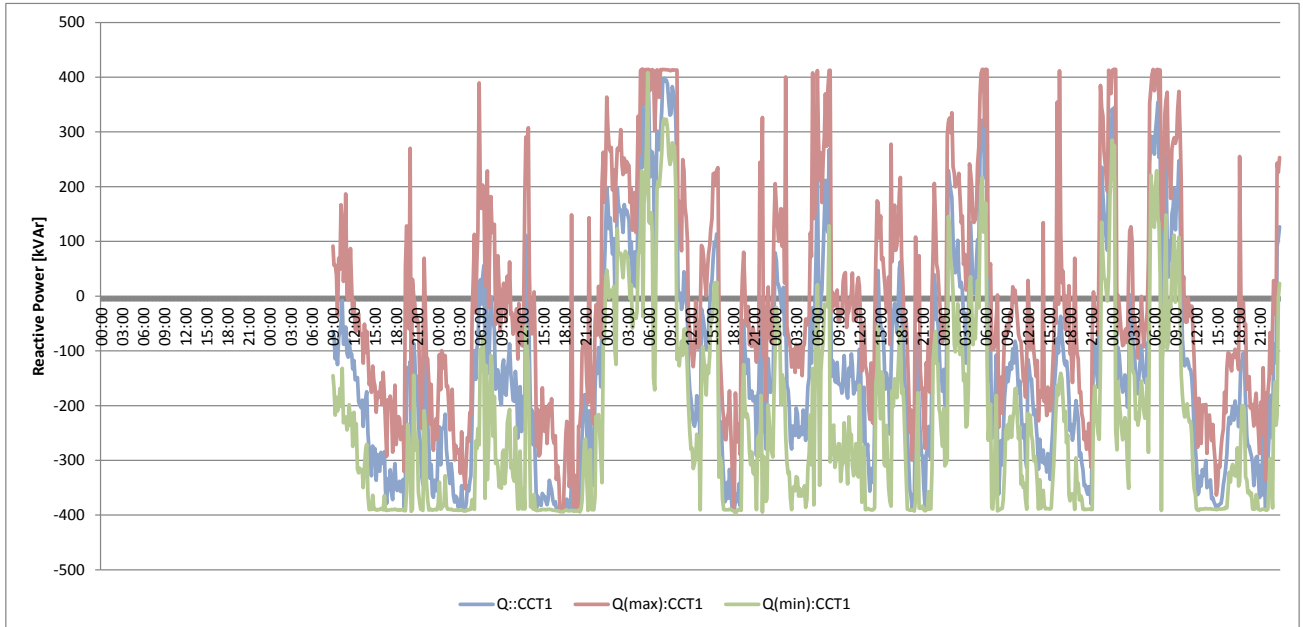


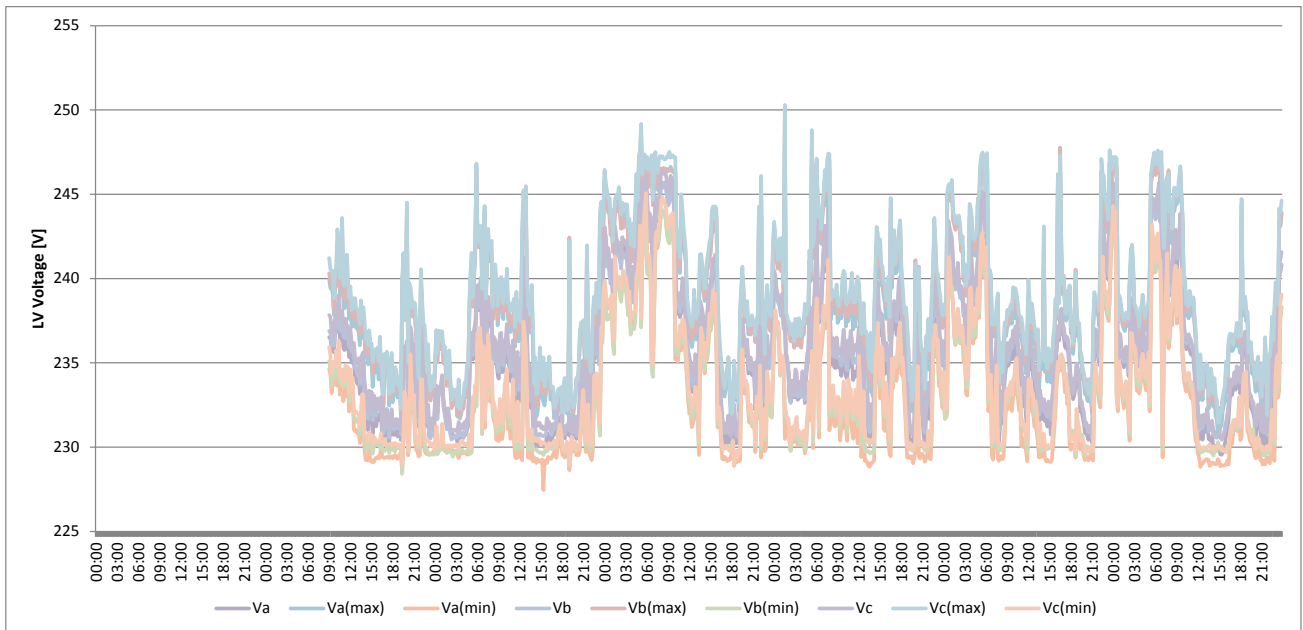
Figure B.3: Calculated Vc at WF during D-SVC off

Appendix C – Summarised weekly low resolution data

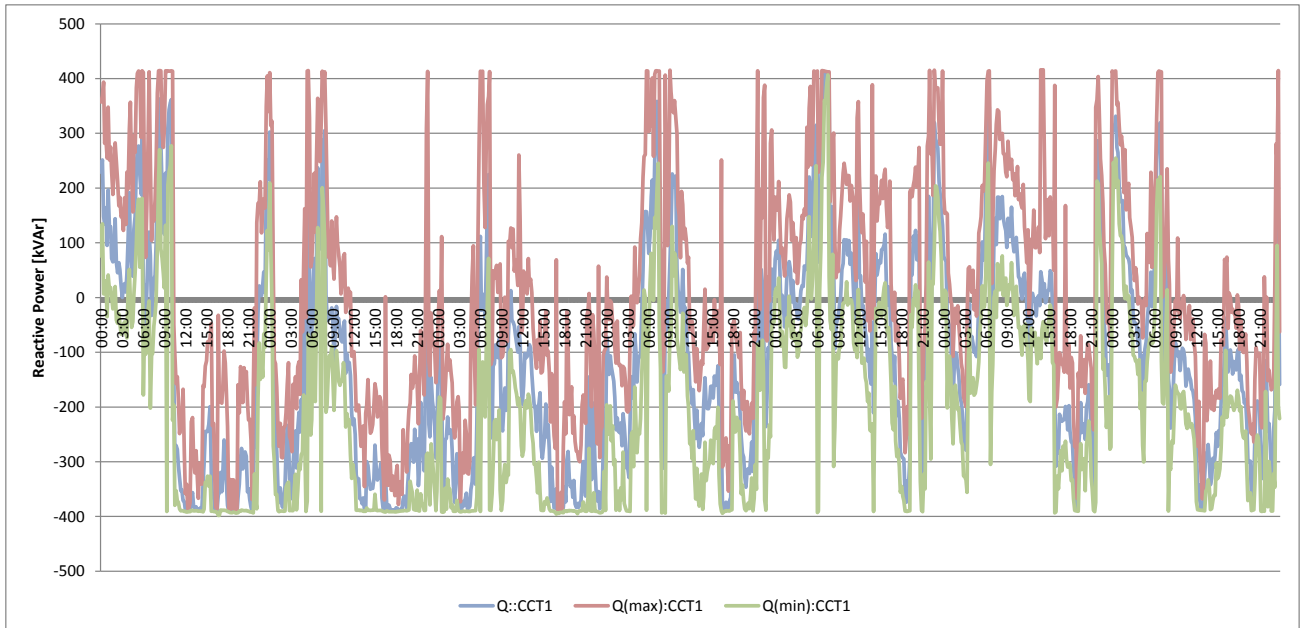
(1) D-SVC



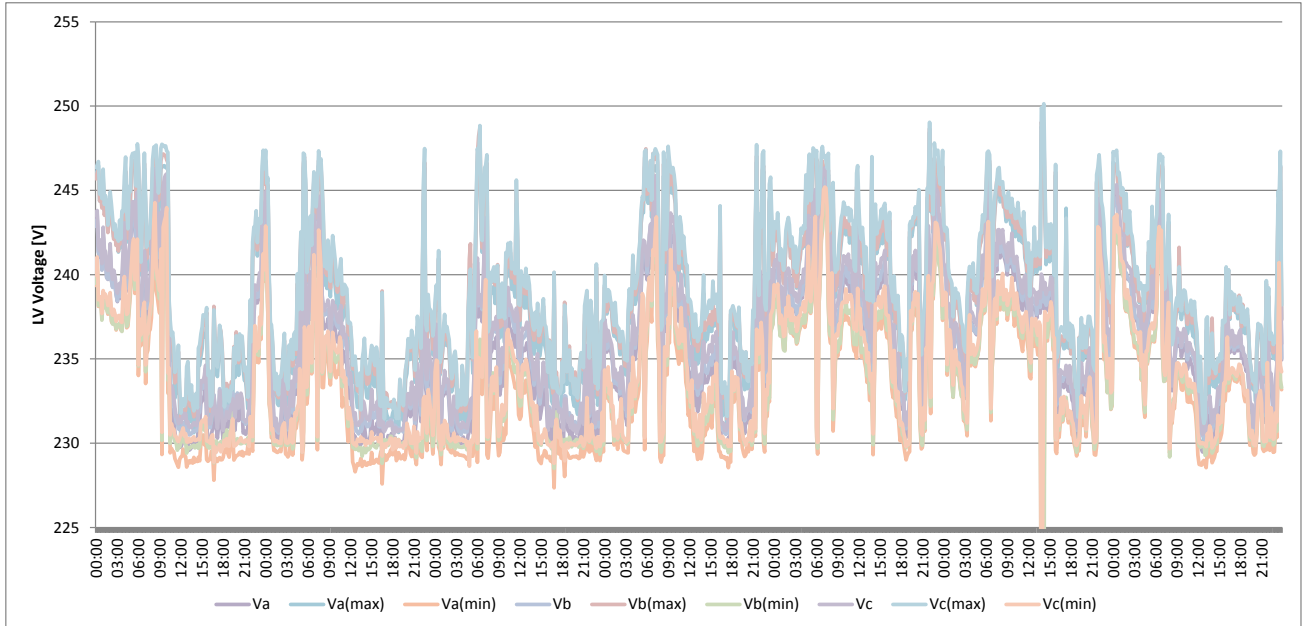
Q recorded from D-SVC SS sub.net 9th – 15th July



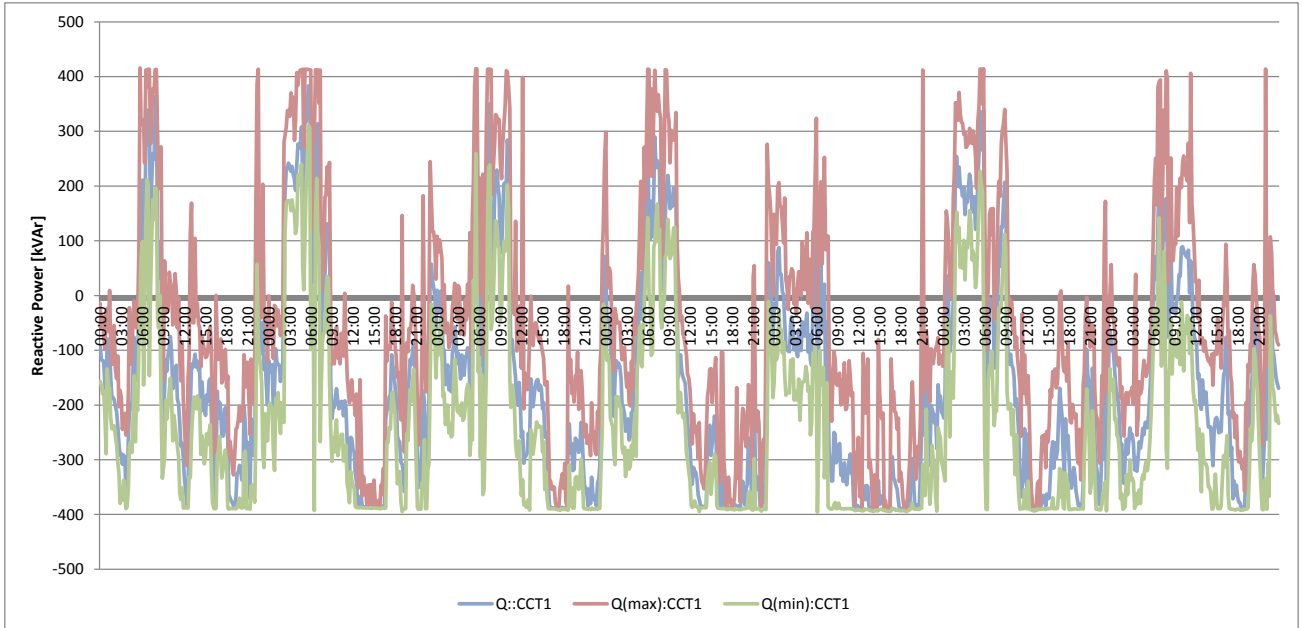
V recorded from D-SVC sub.net 9th – 15th July



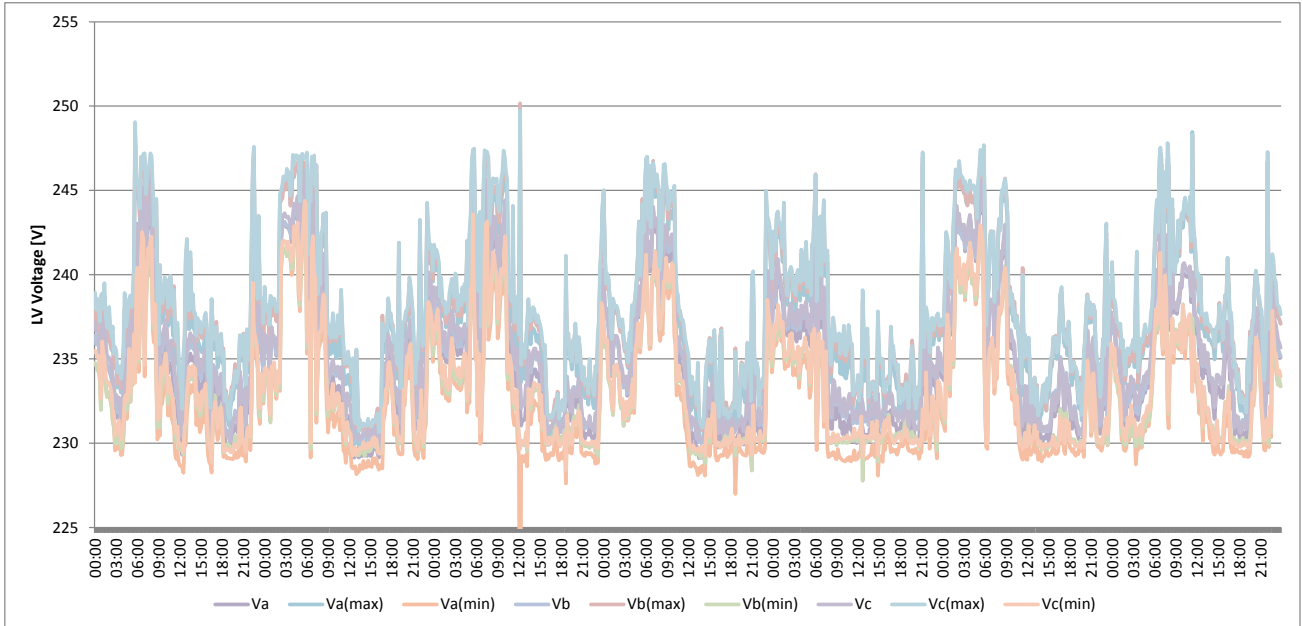
Q recorded from D-SVC sub.net 16th – 22nd July



V recorded from D-SVC sub.net 16th – 22nd July

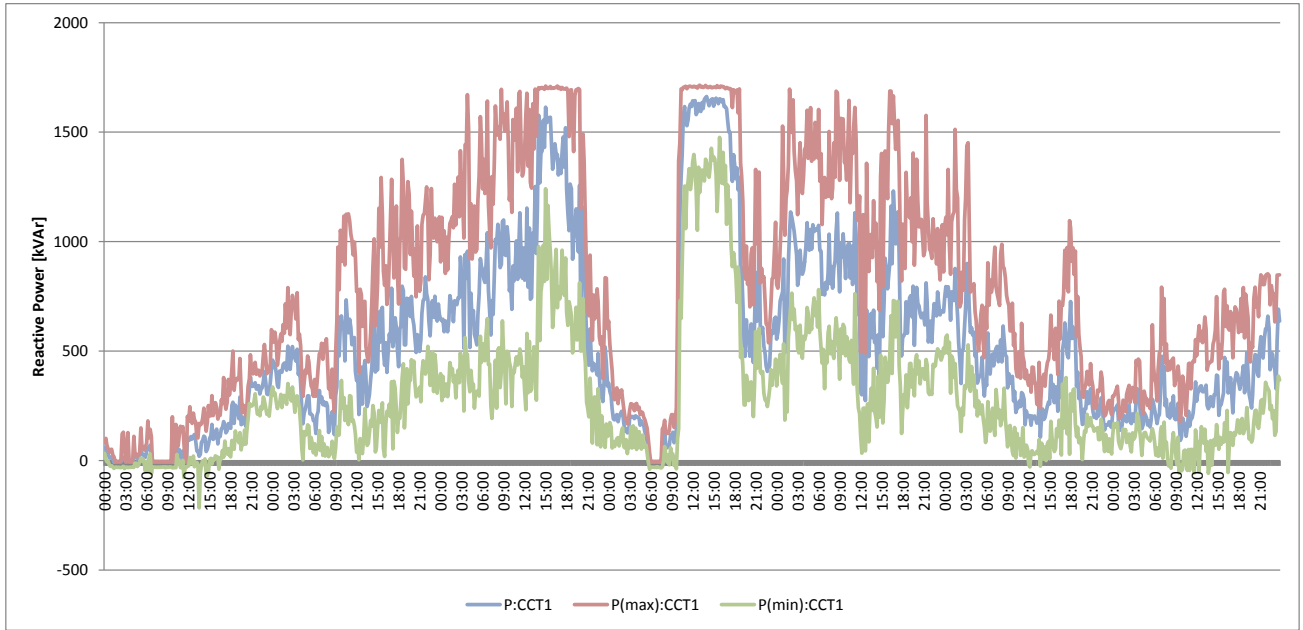


Q recorded from D-SVC sub.net 23rd – 29th July

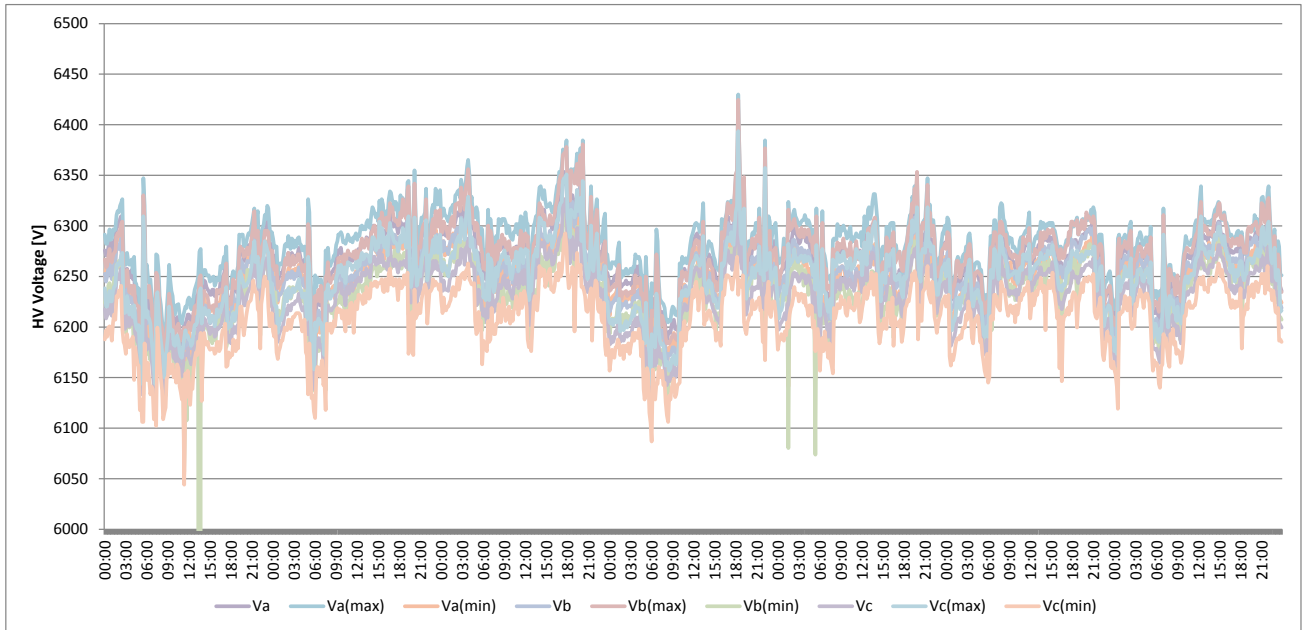


V recorded from D-SVC sub.net 23rd – 29th July

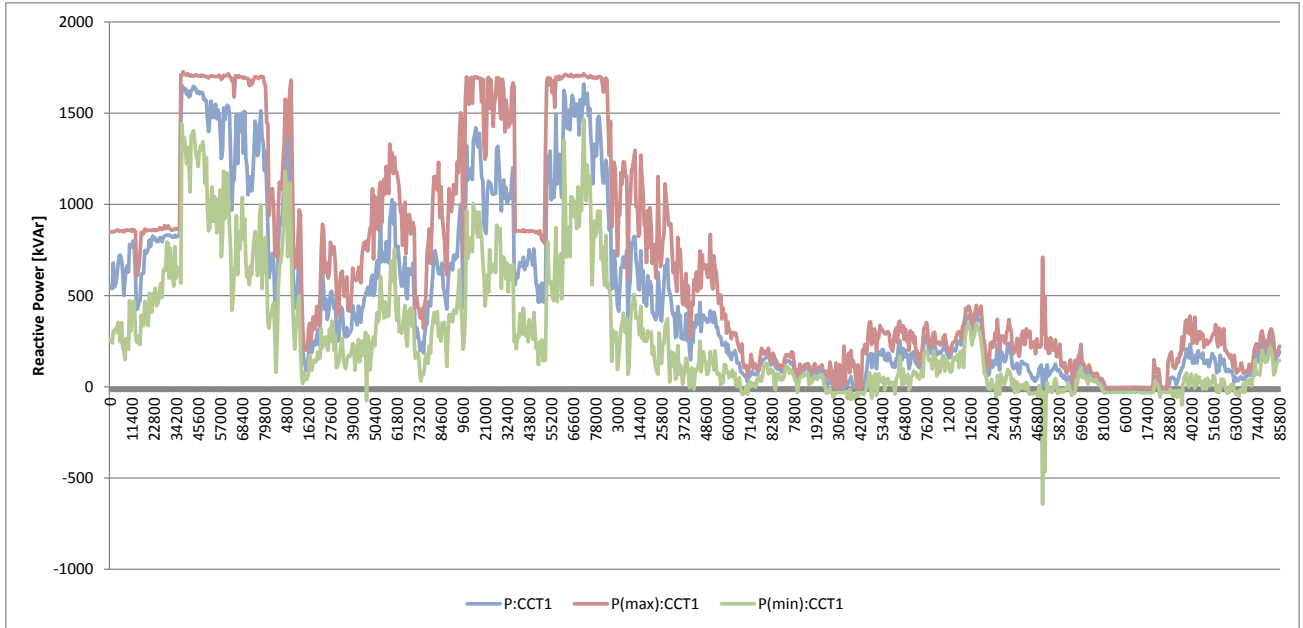
(2) Roskrow WF



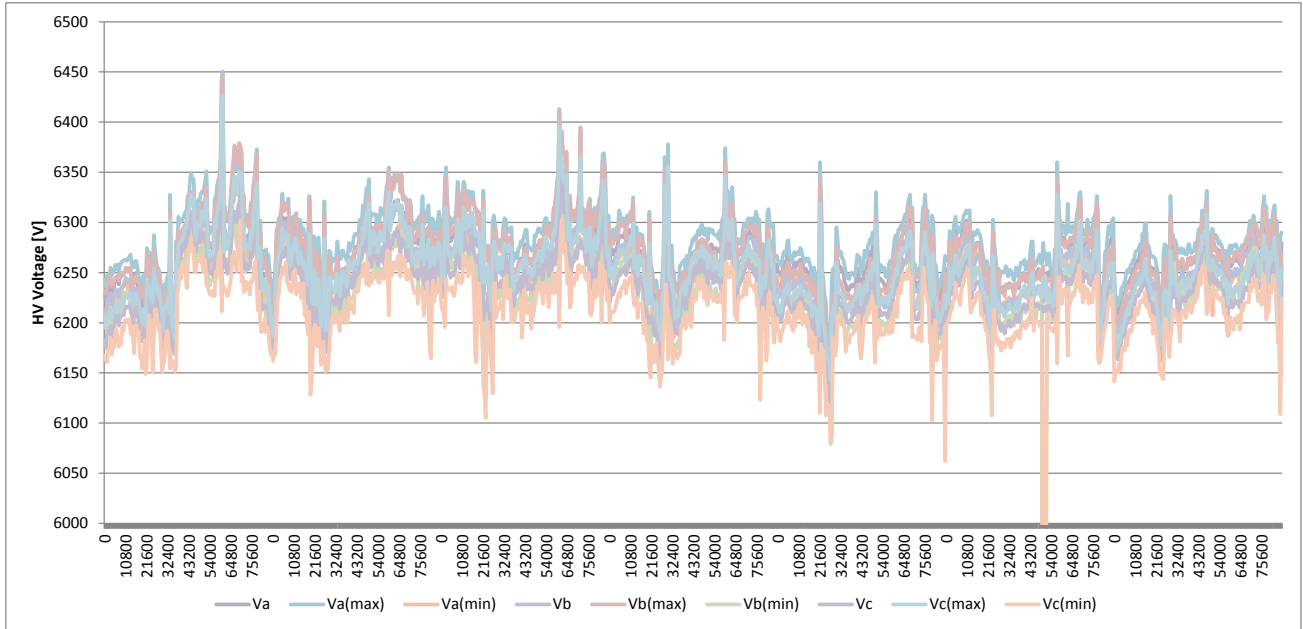
P recorded from Roskrow WF sub.net 9th – 15th July



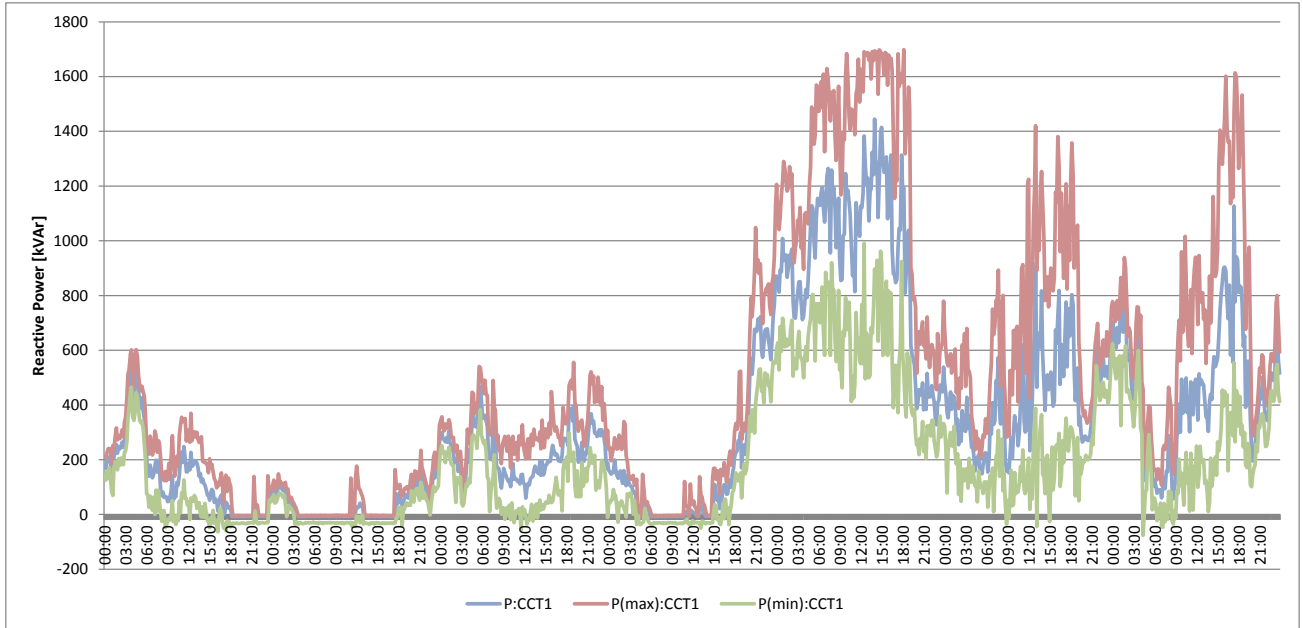
V recorded from Roskrow WF sub.net 9th – 15th July



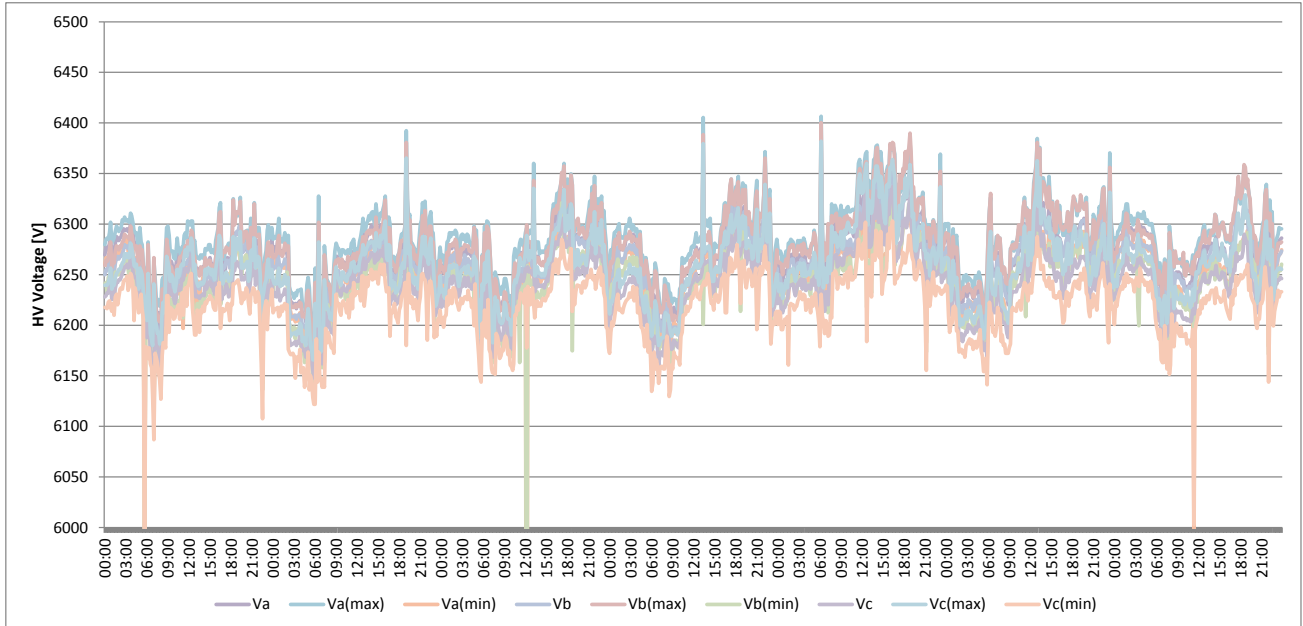
P recorded from Roskrow WF sub.net 16th – 22nd July



V recorded from Roskrow WF sub.net 16th – 22nd July

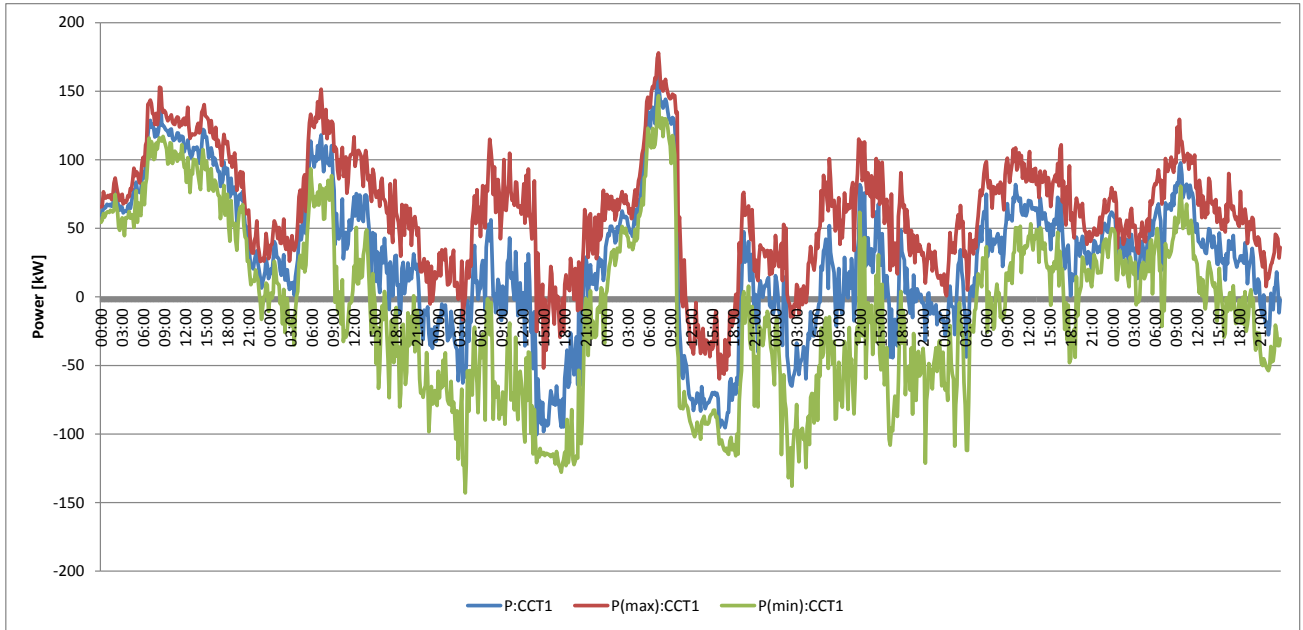


P recorded from Roskrow WF sub.net 23rd – 29th July

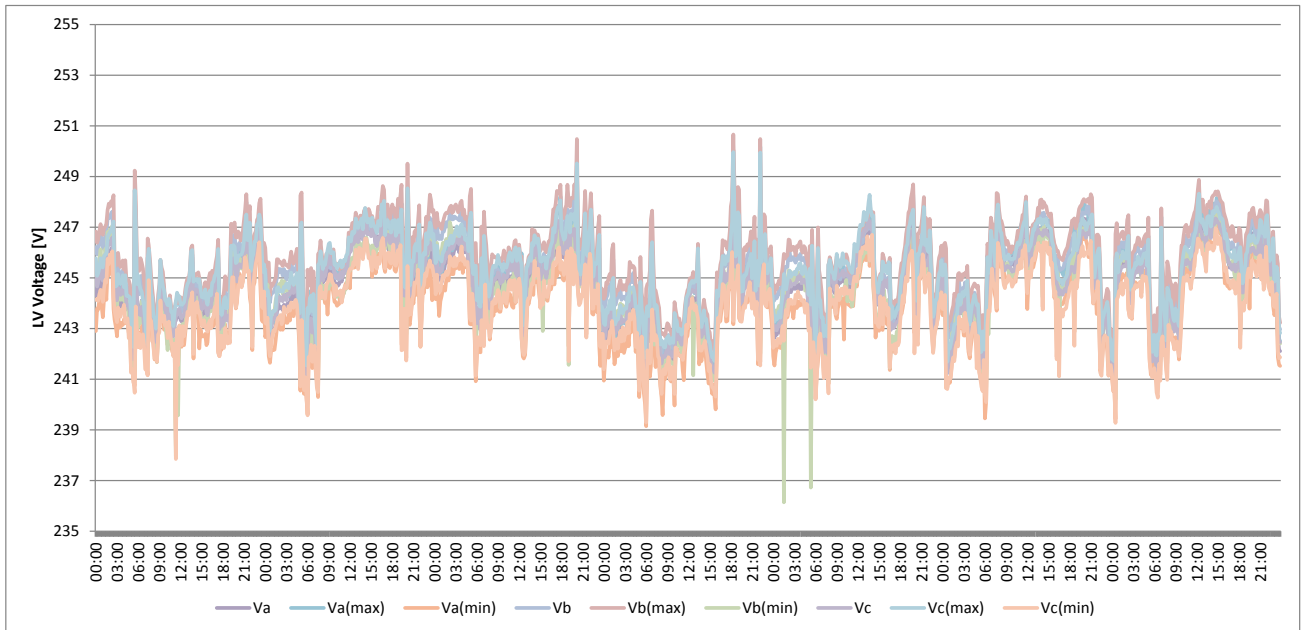


V recorded from Roskrow WF sub.net 23rd – 29th July

(3) Bickland Hill SS



P recorded from Bickland Hill SS sub.net 9th – 15th July

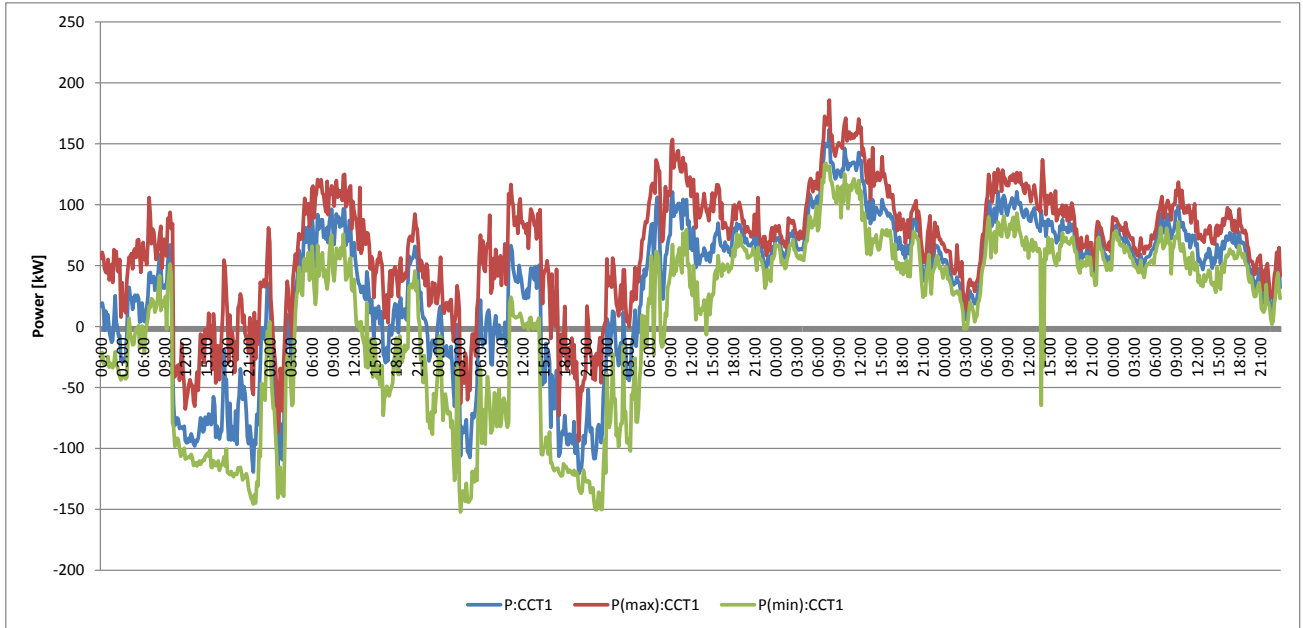


V recorded from Bickland Hill SS sub.net 9th – 15th July

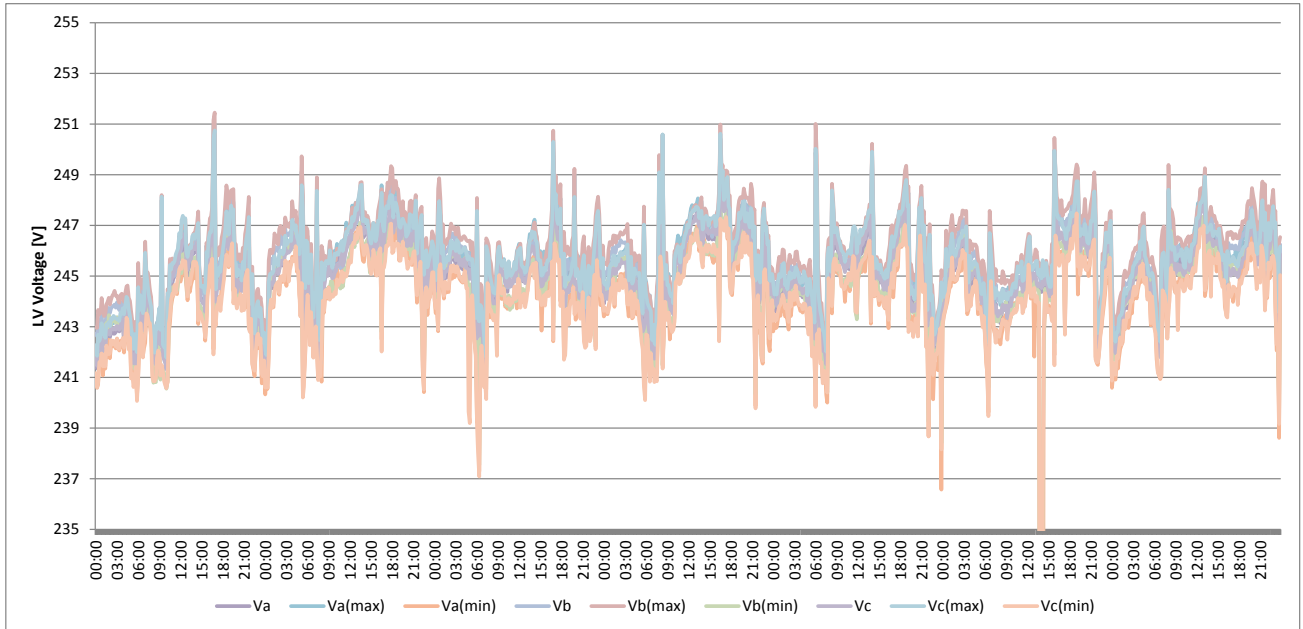
Voltage Control System Demonstration Project Phase 1 – Testing of a D-SVC
Report for D-SVC operation in AVR mode (9th July – 1st August 2012)

Prepared by Hitachi

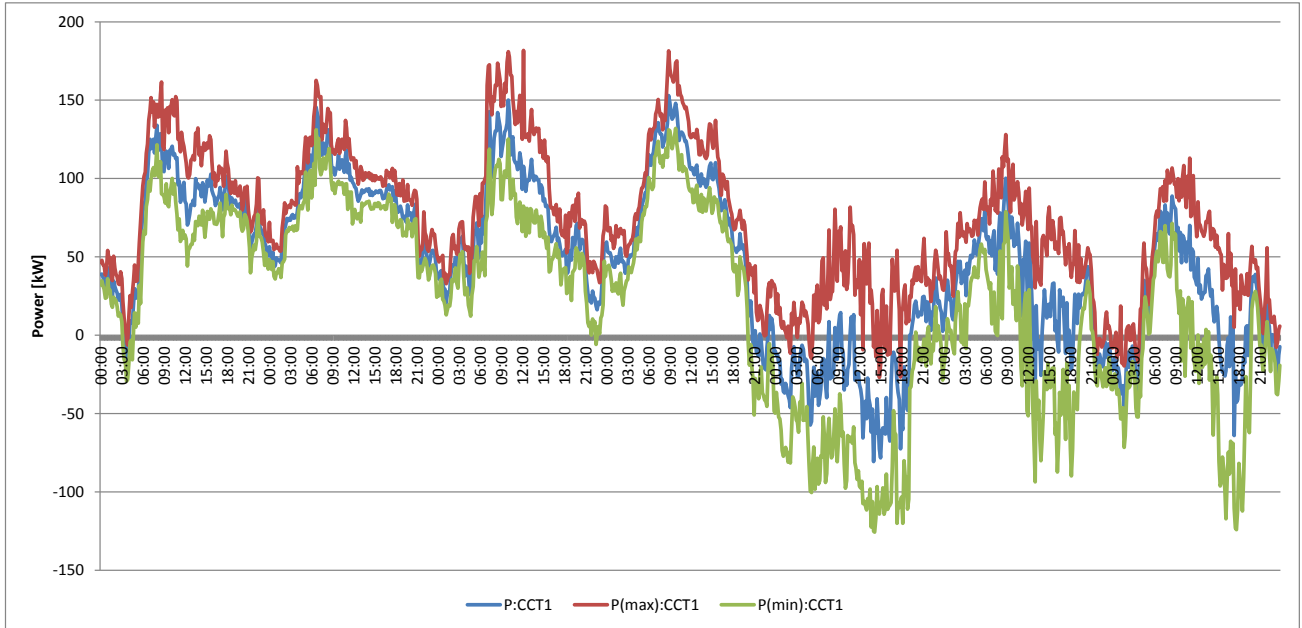
30th August 2012 – Revision 01



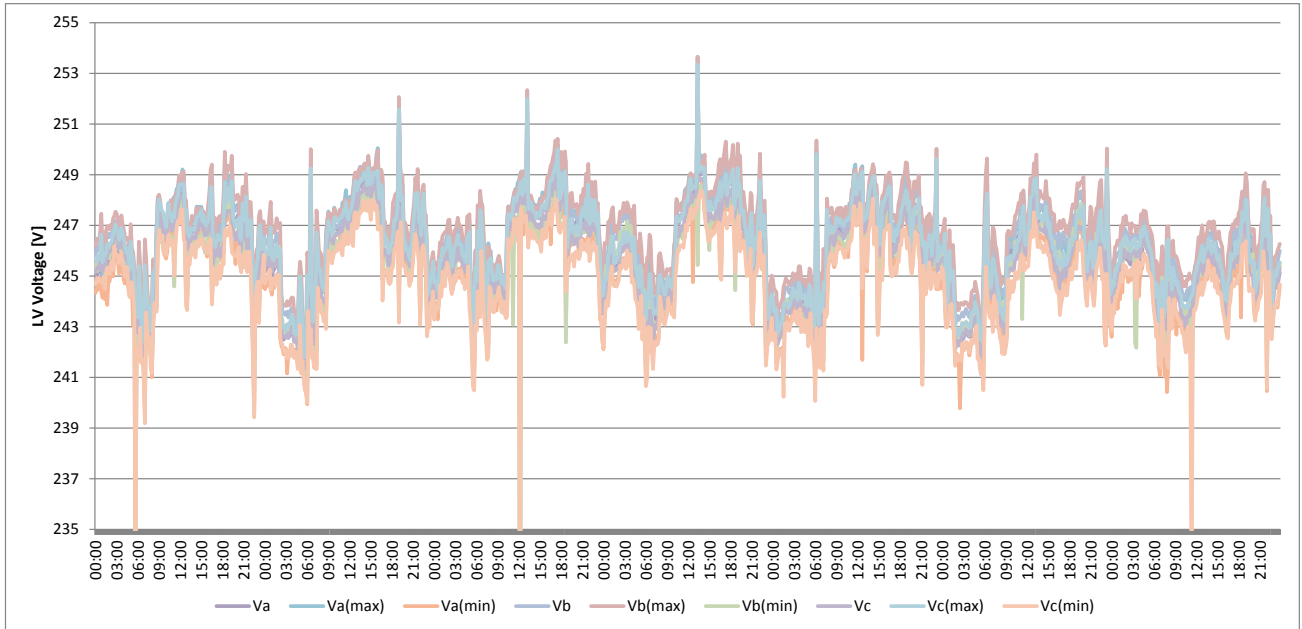
P recorded from Bickland Hill SS sub.net 16th – 22nd July



V recorded from Bickland Hill SS sub.net 16th – 22nd July

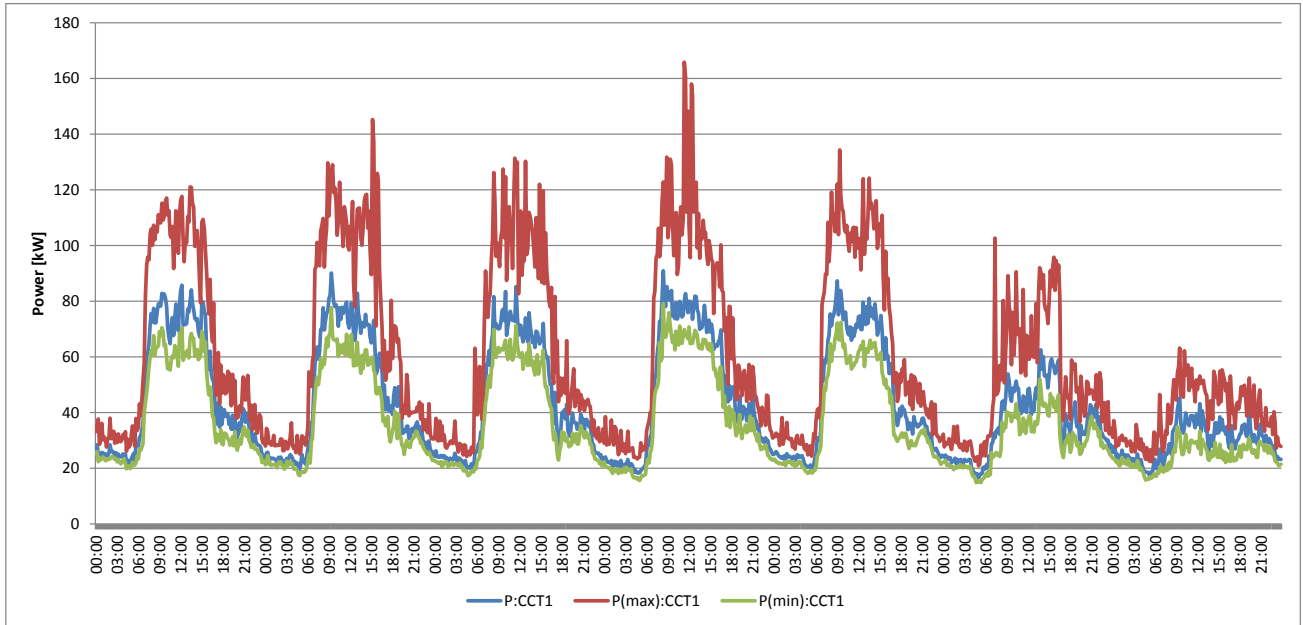


P recorded from Bickland Hill SS sub.net 23rd – 29th July

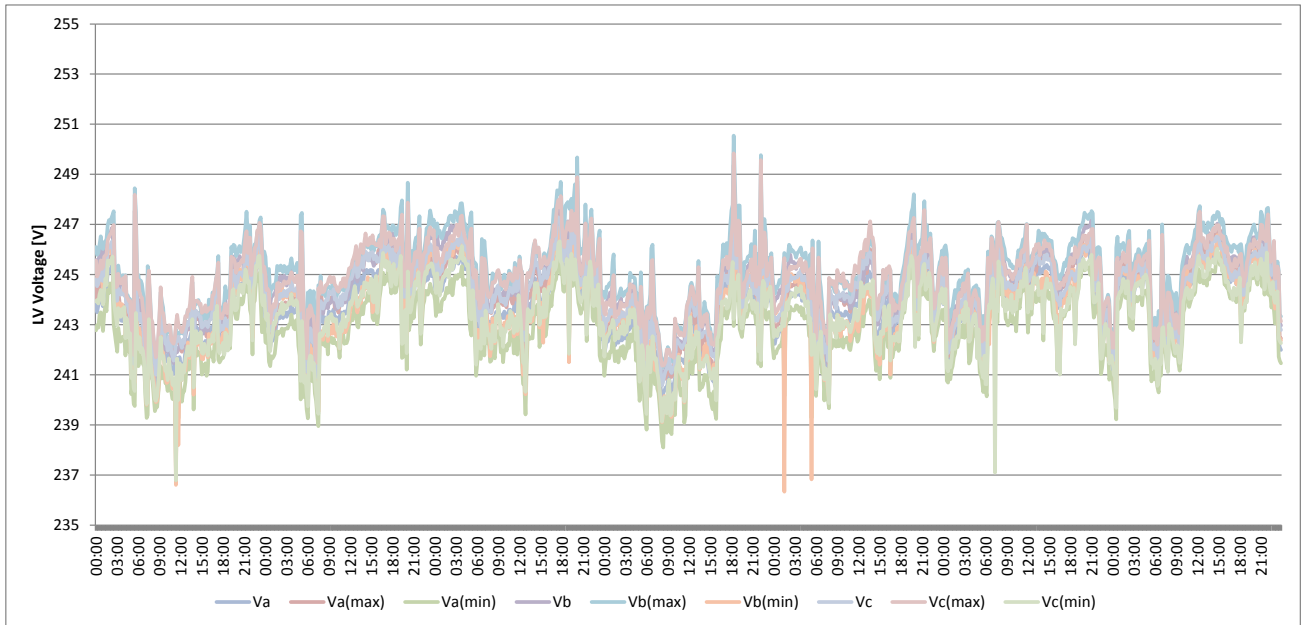


V recorded from Bickland Hill SS sub.net 23rd – 29th July

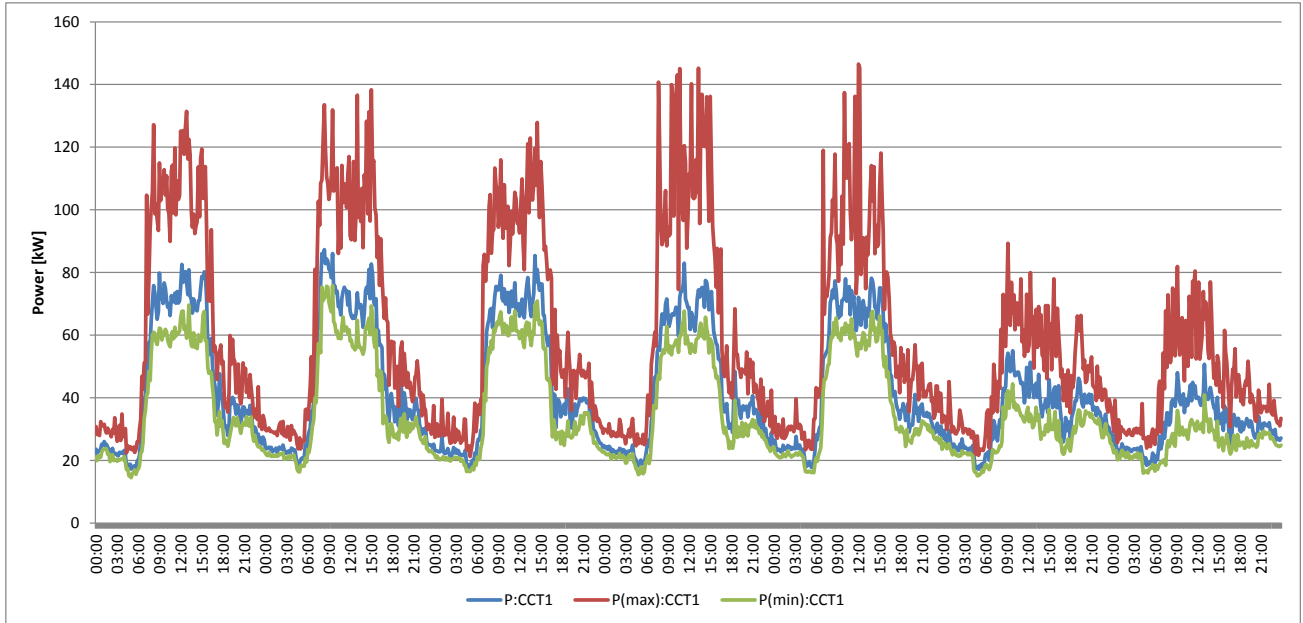
(4) Kernick Ind Est East



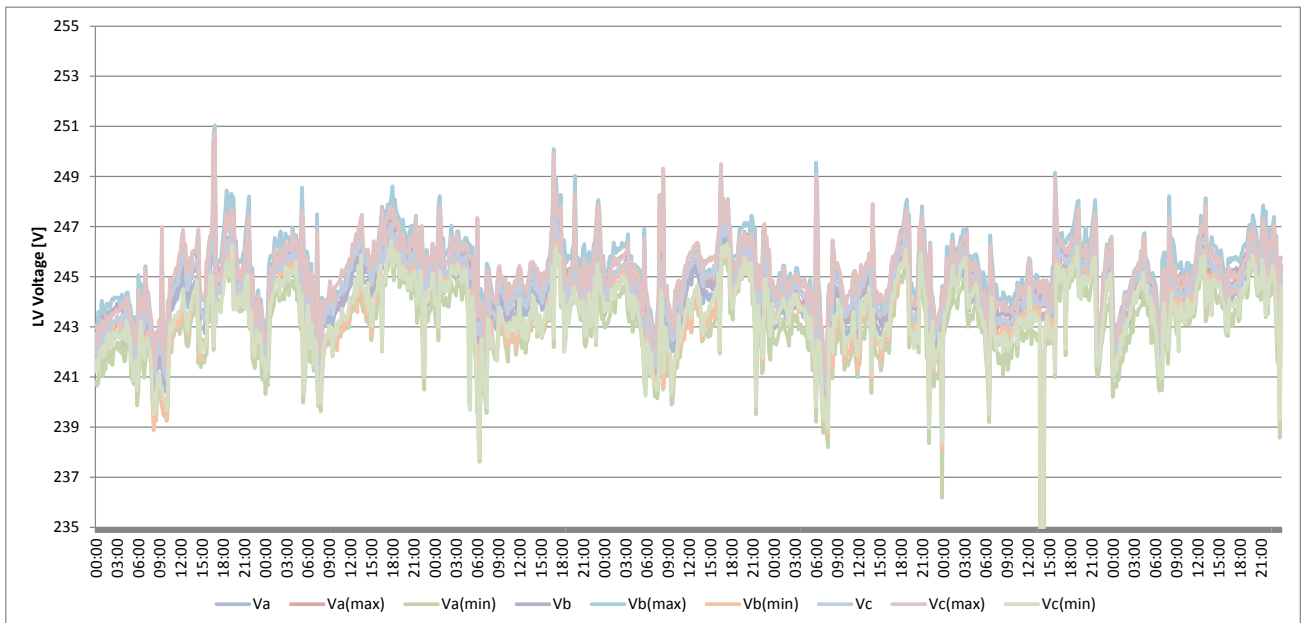
P recorded from Kernick Industrial Estate East sub.net 9th – 15th July



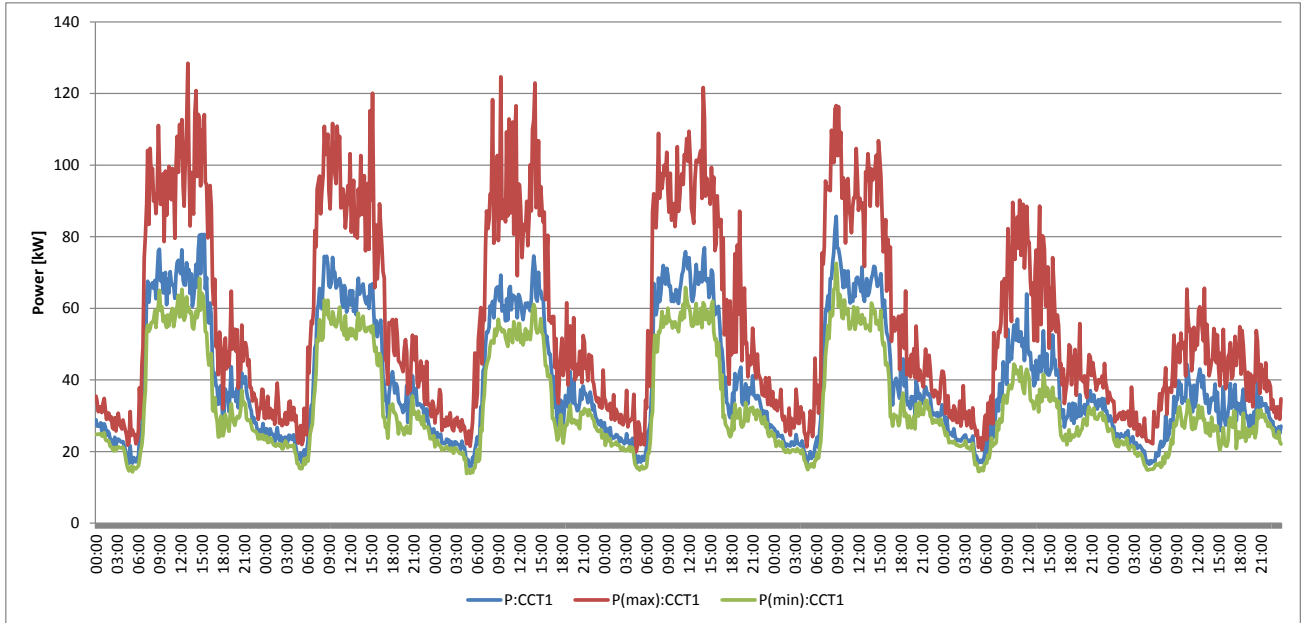
V recorded from Kernick Industrial Estate East sub.net 9th – 15th July



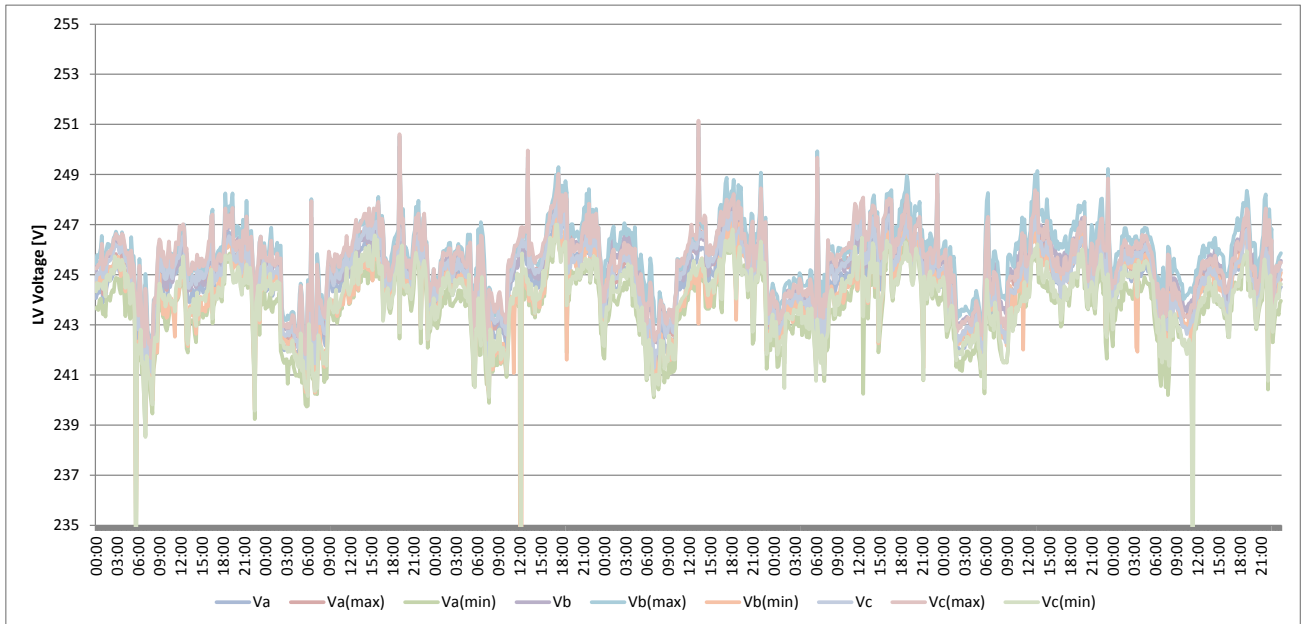
P recorded from Kernick Industrial Estate East sub.net 16th – 22nd July



V recorded from Kernick Industrial Estate East sub.net 16th – 22nd July

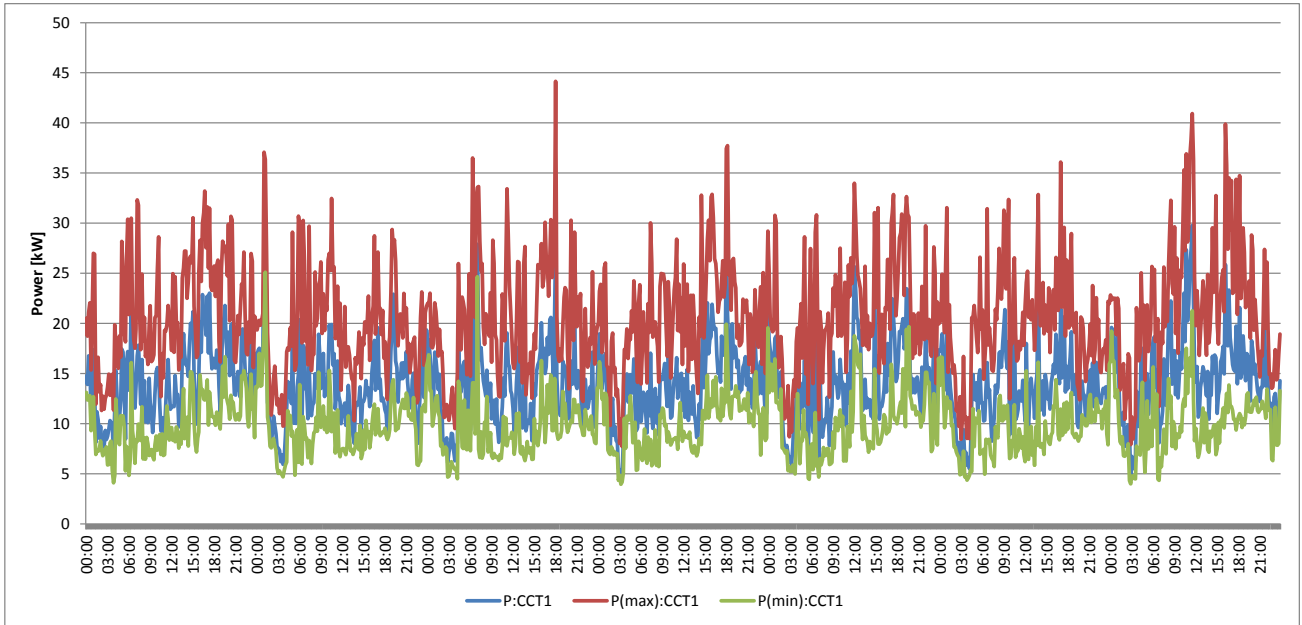


P recorded from Kernick Industrial Estate East sub.net 23rd – 29th July

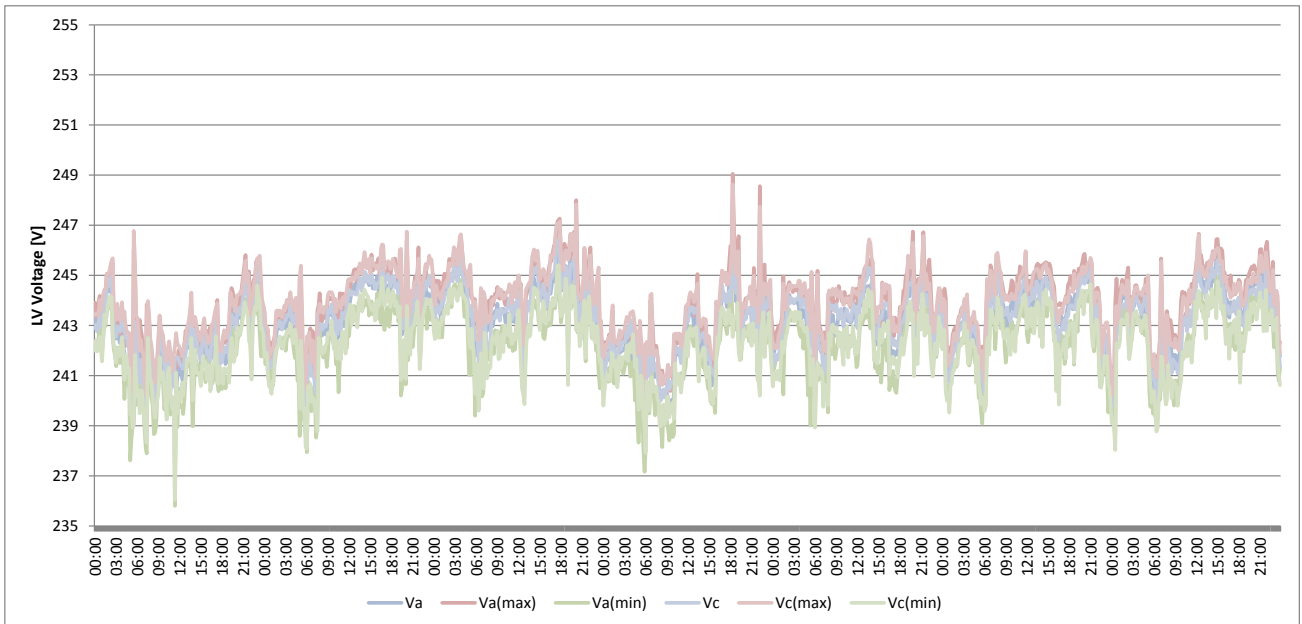


V recorded from Kernick Industrial Estate East sub.net 23rd – 29th July

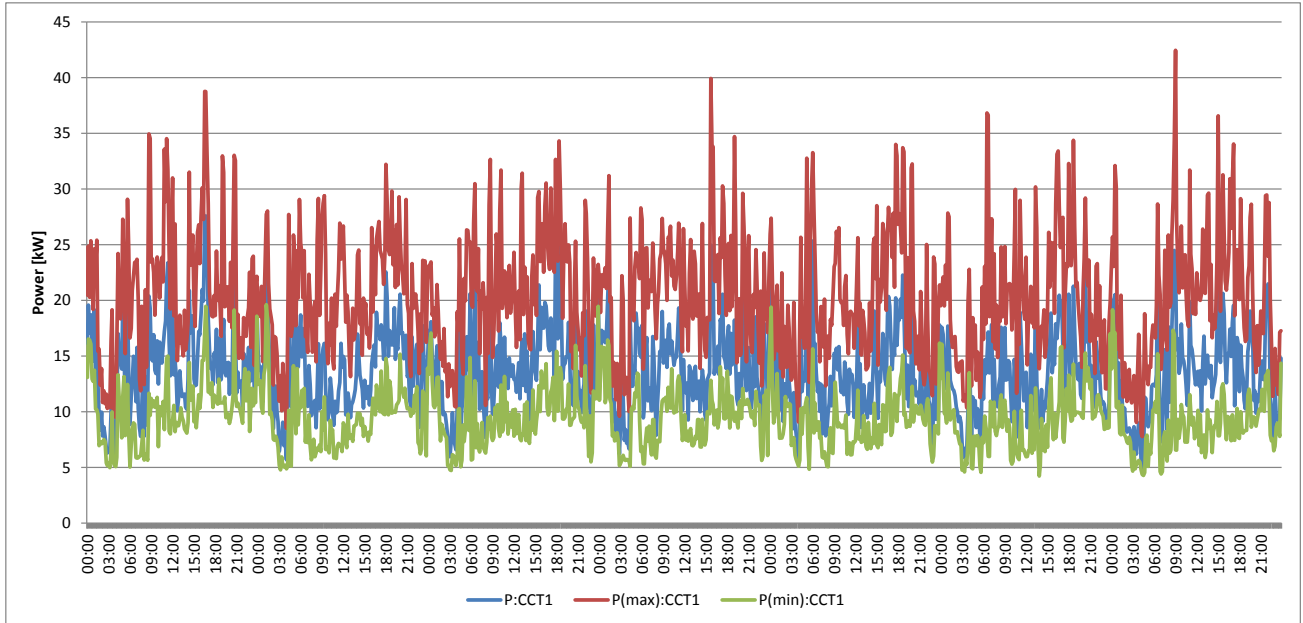
(5) Summerheath



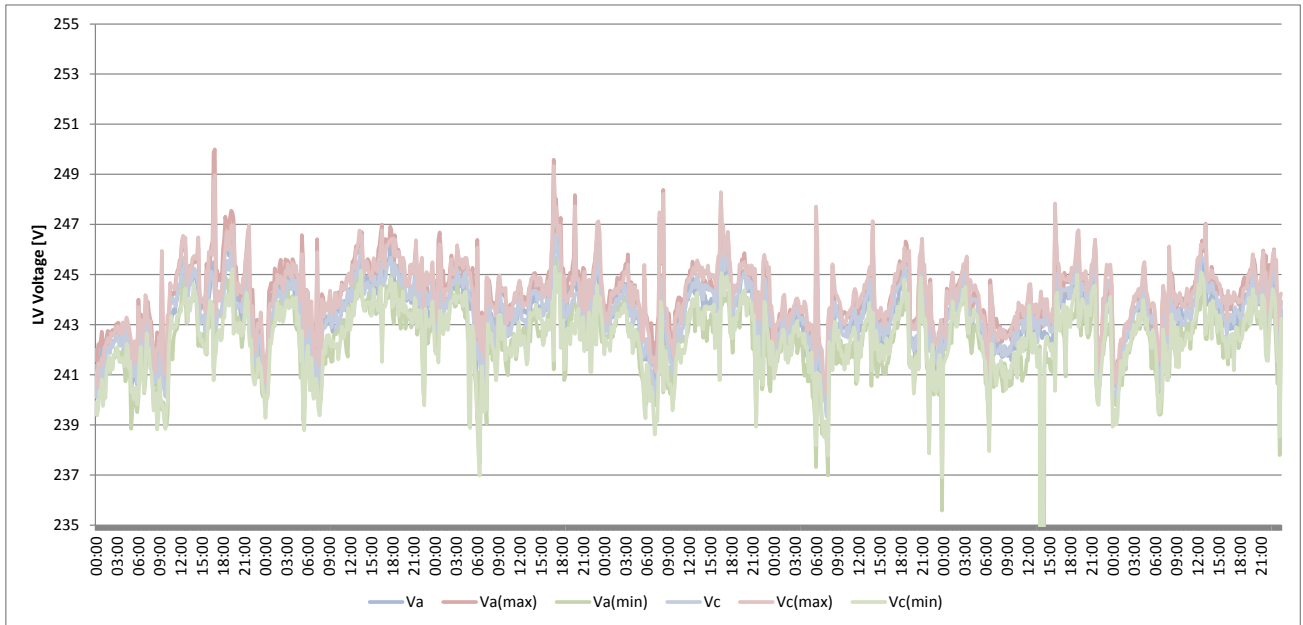
*P recorded from Summerheath sub.net 9th – 15th July
 (Note: data only shows 2 phases due to blown fuse on Vb)*



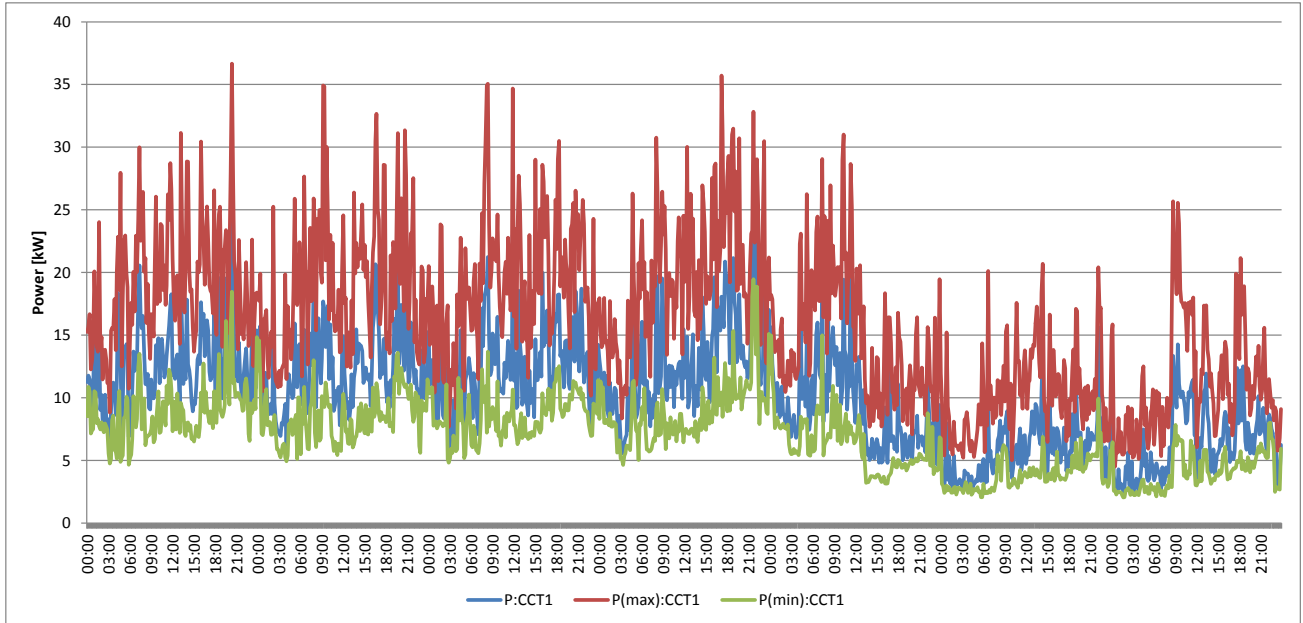
*V recorded from Summerheath sub.net 9th – 15th July
 (Note: data only shows 2 phases due to blown fuse on Vb)*



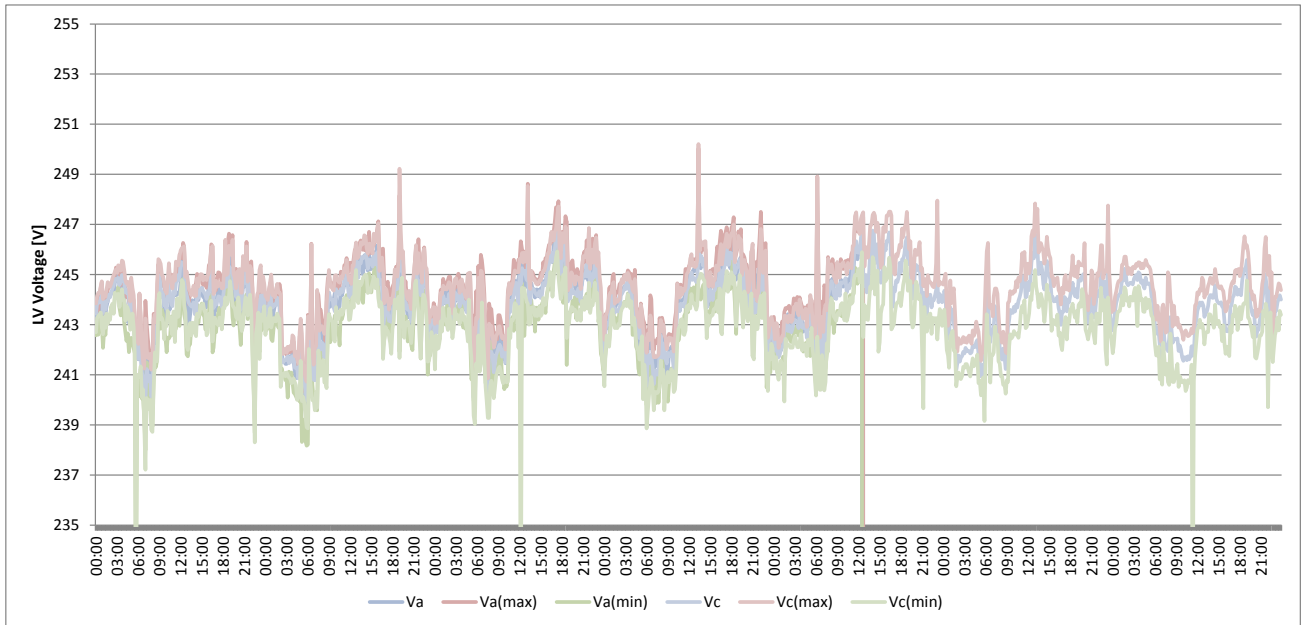
*P recorded from Summerheath sub.net 16th – 22nd July
 (Note: data only shows 2 phases due to blown fuse on Vb)*



*V recorded from Summerheath sub.net 16th – 22nd July
 (Note: data only shows 2 phases due to blown fuse on Vb)*



*P recorded from Summerheath sub.net 23rd – 29th July
 (Note: data only shows 2 phases due to blown fuse on Vb)*



*V recorded from Summerheath sub.net 23rd – 29th July
 (Note: data only shows 2 phases due to blown fuse on Vb)*